CLRCL Full Adder based Low Power Multiplier Architectures

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ABSTRACT

The performance analysis of various multiplier architectures are compared in terms of power, area, delay in the view of low power applications. In this paper, design of array multiplier, Baugh-Wooley multipliers and Braun Multiplier are presented by using CLRCL (Complementary & Level Restoring Carry Logic) Adder. The multipliers presented in this paper were all simulated for 4 bit data. The comparison is made on the basis of Power consumption. To design an efficient integrated circuit in terms of power and area has become a challenging task in modern VLSI design field. In this work, multipliers are designed by using CLRCL Adder and gives better area minimization compared to multipliers using Conventional full adder. Tanner EDA tool was used for simulating designs in the 250nm technologies.

Keywords: Array Multiplier, Baugh Wooley Multiplier, Braun Multiplier, Low Power, VLSI.

I. INTRODUCTION

Multipliers are basic arithmetic operations used in virtually all applications involving digital signal processing. Early multiplier designs focus on pursuing high speed operation or low circuit complexity. However, with the advance of VLSI technology, the computation speed can be improved at a constant pace. Instead, power/energy consumption has become a more and more prominent design factor under the prevailing of battery operated mobile devices. Binary Multiplier is one of the most commonly used circuits in the digital devices. Multiplication is an important arithmetic operation. Most high performance DSP (Digital Signal Processing) systems rely on hardware multiplication to achieve high data throughput. There are various types of multipliers available depending upon the application in which they are used. Previously the main challenge for IC designer was to reduce area of chip. Then the next Demand is to increase the speed of process to attain fast calculations. However area and speed are two conflicting constraints. Now, as most of today’s electronic products are portable, that requires more battery backup. Therefore, lot of research is going on to reduce power consumption. So, in this paper it is tried to find out the best solution to achieve low power consumption for multiplier operation.

II. PREVIOUS WORK

Conventional CMOS full adder in Figure.1 with 28 transistors is a high power and high performance full adder, which has been designed, based on CMOS topology. It has full-swing outputs that increase reliability. Due to high number of transistors its power consumption is high. Large PMOS transistor in pull up network result in high input capacitances, which cause high delay and dynamic power and using inverters on the output nodes, decreases the rise-time and fall-time.

![Fig.1: Conventional CMOS Full Adder](image)

By using conventional CMOS full adder various multiplier architectures are designed. In terms of power, area occupation and delay, those multipliers are inefficient for digital signal processing applications.

III. CLRCL (COMPLEMENTARY & LEVEL RESTORING CARRY LOGIC) FULL ADDER

The equation of Complementary and Level Restoring Carry Logic (CLRCL) full-adder is shown as below:

\[
Sum = (A \oplus B).Cout + (A \oplus Cin).B
\]

\[
Carry = (A \oplus Cin).B + (A \oplus Cin).A
\]

The Complementary and level restoring carry logic full-adder is a low complexity circuit, so as to obtain faster cascade operation. Proper level restoring technique with the inverter is used to solve the multiple threshold...
Voltage fit losses problem in the carry propagate chain [9]. The XNOR circuit adopted in the design is realized by a 2-to-1 multiplexer followed by an inverter as shown in figure 2. The function of the inverter is 3-fold. Firstly, it is used as a level restoring circuit to contest the output threshold voltage loss. The level restored output is then fed to MUX 2/3 to produce Sum and Carry signals. The threshold voltage loss of Sum and Carry will be restricted to only one away from the power supplies. Secondly, the inverter serves as a buffer along the carry chain to speed up the carry propagation. Thirdly, the inverter provides complementary signals needed in the following stage.

![Fig. 2: CLRCL Full Adder](image)

The availability of complementary signals also helps simplify the XNOR design, where only one signal is needed in selection control [4]. In order to rectify the defects in the SERF adder the 10T CLRCL Full adder was introduced. The main aim of the design is that the carry signal must not suffer from distortion as it propagated. The circuit diagram of 10T CLRCL full adder is shown in Figure 2. It consists of two transistor xor structures. The inverters used prevent threshold loss problem and propagate the full swing signals to generate the carry. Though the carry signal has full swing operation, this circuit consumes more power.

IV. MULTIPLIER ARCHITECTURES

Digital multiplication is one of the most basic functions in a wide range of algorithms [12]. The ubiquity of this operation in computing has given rise to a large number of multiplier implementations, each with different specifications and goals. Some applications require wide dynamic range, others need high precision, while in some cases, neither of these characteristics are very tightly specified. Digital multiplication is used as opposed to analog when high precision is an issue; it is fairly straightforward to make digital multipliers as accurate as the application requires. Precision required for multiplication varies by function. At the low end, 8 bits are needed, e.g., in image compression algorithms, or 16 bits in more precise DSP tasks. At the high end, we see 53 bit and 64 bit multiplication. Typically, we see 16 bit multipliers used for digital signal processing and 53/64 bit multipliers used in microprocessors.

The basic operation in these designs is integer multiplication; in floating point multipliers, integer multiplication units are sub-blocks of the greater floating point unit. Signed versus unsigned techniques have an impact on the design, and some clever techniques have been suggested for manipulating the bit representation of numbers to generate power savings. However, the primary consideration in multipliers has been and continues to be delay. Generally Digital multiplication consists of two basic steps, these are:-

1. Evaluation of partial product
2. Accumulation of the shifted partial product

It should be noted that binary multiplication is equivalent to logical AND operation. Thus evaluation of partial products consists of logical ANDing of the multiplicand and the relevant multiplier bit. There are a number of techniques that may be used to perform multiplication. In general, the choice is based upon factors such as speed, throughput, numerical accuracy, area.

A. Multiplier Structure

At the most basic level, digital multiplication can be seen as a series of bit shifts and bit additions, where two numbers, the multiplier and the multiplicand are combined into the final result. Consider the multiplication of two numbers: the multiplier P, and multiplicand C, where P is an n-bit number with bit representation \(\{p_{n-1}, p_{n-2}, ..., p_0\}\), the most significant bit being \(p_{n-1}\) and the least significant bit being \(p_0\); C has a similar bit representation \(\{c_{n-1}, c_{n-2}, ..., c_0\}\). For unsigned multiplication, up to n shifted copies of the multiplicand are added to form the result. The entire procedure is divided into three steps: partial product (PP) generation, partial product reduction, and final addition. This is illustrated conceptually in Fig. 3.

B. Array Multiplier

The array multiplier originates from the multiplication parallelogram. Each stage of the parallel adders should receive some partial product inputs. The carry-out is propagated into the next row. In array multiplier, all of the partial products are generated at the same time. It is observed that the critical path consists of two parts: vertical and horizontal. Both have the same delay in terms of full adder delays and gate delays. For an n-bit by n-bit
array multiplier, the vertical and the horizontal delays are both the same as the delay of an n-bit full adder. One advantage of the array multiplier comes from its regular structure.

Fig.3. Digital multiplication flow.

Since it is regular, it is easy to layout and has a small size. The design time of an array multiplier is much less than that of a tree multiplier. A second advantage of the array multiplier is its ease of design for a pipelined architecture. A fully pipelined array multiplier with a stage delay equal to the delay of a 1-bit full adder plus a register has been successfully designed for high speed DSP applications [7], [2]. In Array multiplier, almost identical calls array is used for generation of the bit-products and accumulation. All bit-products are generated in parallel and collected through an array of full adders or any other type of adders and final adder. Array multiplier has a regular structure that simplifies the wiring and the layout. Therefore, among other multiplier structures, array multiplier takes up the least amount of area but it is also the slowest with the latency proportional to $O(W_d)$ where $W_d$ is the word length of the operand.

C. Baugh-Wooley Multiplier

The Baugh-Wooley (BW) algorithm is a relatively straightforward way of doing signed multiplications. The creation of the reorganized partial-product array comprises three steps: The most significant bit (MSB) of the first $N-1$ partial-product rows and all bits of the last partial-product row, except its MSB, are inverted. A ‘1’ is added to the Nth column. The MSB of the final result is inverted [2].

D. Braun multiplier

Braun multiplier is an uncomplicated parallel multiplier generally called as carry save array multiplier. The structure consists of array of AND gates and adders arranged in the iterative way and no need of logic registers. This can be called as non-addictive multipliers [2].

In the internal structure, each products can be generated in parallel with the AND gates. Each partial product can be added with the sum of partial product which has previously produced by using the row of adders. The carry out will be shifted one bit to the left or right and then it will be added to the sum which is generated by the first adder and the newly generated partial product.

V. SIMULATION RESULTS

The simulation results for Conventional CMOS Full Adder, CLRCL Full Adder, Array Multiplier, Baugh Wooley Multiplier and Braun Multiplier are Shown Below.

Fig. 4: Conventional CMOS Full Adder

Fig. 5: Output Results for CLRCL Full Adder
Table I: Transistors Count For Full Adders

<table>
<thead>
<tr>
<th>Full Adder Type</th>
<th>No. of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coventional FA</td>
<td>28</td>
</tr>
<tr>
<td>CLRCL FA</td>
<td>10</td>
</tr>
</tbody>
</table>

Table II: Power Comparision of Multiplier Architectures

<table>
<thead>
<tr>
<th>Multiplier Architecture</th>
<th>Power(mW)</th>
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</thead>
<tbody>
<tr>
<td>4x4 Array Multiplier</td>
<td>8.34</td>
</tr>
<tr>
<td>4x4 Baugh Wooley Multiplier</td>
<td>10.2</td>
</tr>
<tr>
<td>4x4 Braun Multiplier</td>
<td>8.87</td>
</tr>
</tbody>
</table>

From the above simulation results and Table I and Table II shows that better in the Multipliers designed by using CLRCL (Complementary & Level Restoring Carry Logic) Adder gives better performance in terms of power consumption and area occupation.

VI. COMPARISON CHART

Chart 1: Transistors Count For Full Adders

Chart 2: Power Comparision of Multiplier Architectures
VII. CONCLUSION

In this paper, we have presented the power characteristics of three different multipliers realized using CLRCL (Complementary & Level Restoring Carry Logic) Full Adder. For comparative analysis, we realized 4x4 Array Multiplier, Baugh Wooley Multiplier and Braun Multiplier. In all the multiplier configurations investigated, the CLRCL Full Adder based multipliers exhibited better area compared conventional full adder based multipliers. Among these three multipliers array multiplier gives better performance in the characteristic of power consumption compared to Baugh Wooley Multiplier and Braun Multiplier.

REFERENCES