FPGA BASED VIDEO INPUT DIRECTION FINDER
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ABSTRACT
In Electronic Warfare, one of the requirements is to find the direction of arrival of analog signals. These analog signals may be video signals. For finding the direction of arrival (DOA), an efficient technique being used is Amplitude Comparison Technique involving normalization and calibration of Amplitude data. Designing of Analog input Direction Finder involves selection of various modules and interfacing it according to the requirement. These modules are programmed and tested using Virtex-5 in Xilinx and EDK simulation tools. This paper discusses about the designing and interfacing of different modules of Analog (video) Input direction finder on FPGA according to the requirement for the electronic warfare

Keywords: Direction of arrival, Normalization, Calibration, FPGA, pulse parameters, Modules, Video Signals.

1. INTRODUCTION
Finding the direction of arrival of the analog signals received is very important in electronic warfare. The input signals are RADAR signals. These are converted to video signals and considered as input signals to the board. The objective of the paper is to design a FPGA based analog input direction finder to determine from which direction the signals are being received and the phase angle of the received signal. The other functions of this design are measurement of pulse parameters like Pulse Width (PW), Pulse Repetition Interval (PRI) & Time of Arrival (TOA) and generation of 32 bit Pulse Descriptor word along with controls. It also generates controls to SP4T (Single –Pole Four Throw) Radio Frequency switch based on maximum signal strength for enabling frequency measurement.

The design of FPGA based direction finder involves interfacing of different modules. These modules are: i. Switch control Section. ii. Analog Interface Section. iii. Comparator Section. iv. Memory Interface Section.

These modules are interfaced as shown in figure 1.

To realize all these functional blocks, DF and Pulse Processor hardware has to be developed and the VHDL code required for implementing the above will be developed and ported on to the FPGA.

2. INTERFACING
2.1. Switch control section:
- This section contains SPST Switches and Video Buffers.
- The SPST switch consists of four individual switches and one control line for each individual switch.
- The Video Buffers are Quad Channel Buffers, used either to amplify or buffer the received video signals. These Video Buffers operate at ±5V.

The switch control section accepts four video signals through the VME interface connector. These video signals are fed to two SPST switches (SW1 and SW2). Each SPST switch accepts two Video signals along with the two BIT_IN signal from the DAC. Each video signal is tied up with BIT_IN signals at the output of the SPST switch and controlled by the control inputs {Sw_VB(0:7)} from the FPGA, so that the SPST switch can function as an SPDST switch.
The output from the SPDT switch is fed to a video buffer (BUF_1). Output of the BUF_1 is given to two SPDT switches (SW3 and SW4) and also to COMP_3 in COMPARATOR Section as shown in figure 3. The SW3 and SW4 accepts the AC coupled and DC coupled inputs from the outputs of BUF_1 and controlled by SW_C signals from the FPGA.

The output of SW3 and SW4 are fed to video amplifiers/buffers BUF_2, BUF_3 and BUF_4. The outputs from BUF_2, BUF_3 and BUF_4 are (N1, S1, E1, W1), (N2, E2, S2, W2) and (N3, E3, S3, W3) respectively. The (N1, S1, E1, W1), (N2, E2, S2, W2) are fed to COMPARATOR SECTION and (N3, E3, S3, W3) are fed to ANALOG INTERFACE SECTION for further processing.

2.2. Comparator Section:
- This section consists of comparators, Level Translators and DACs.
- These comparators are dual channel comparators operating at +5V.
- The Level translators converts the TTL inputs to LV TTL outputs and vice-versa. These 16 bits are divided into groups of 8 bits with separate controls for each.
- DAC is a complete voltage output 8-bit digital to analog converter and includes a output voltage amplifier. The DAC operates on +5V single supply and is configured to generate a maximum full scale voltage ranging from +0V to +2.56V. This implies that each bit is capable of generating 12mV. The 8-bit Input to the DAC is derived from the FPGA.

The Video buffer outputs from the Switch Control section are fed to comparators in the comparator section. The Video buffer BUF_1 outputs (N, S, E, W) are fed to COMP_1 (Two comparators) and a threshold voltage derived from the DAC is also fed to COMP_1. The TTL outputs of the COMP_1 are driven to Level Translators and LV TTL outputs of the Level Translators are fed to FPGA.

The Video buffer BUF_3 outputs (N1, S1, E1, W1) are fed to COMP_3 (Two comparators) and a threshold voltage derived from the DAC is also fed to COMP_3. The TTL outputs of the COMP_3 are driven to Level Translators and LV TTL outputs of the Level Translators are fed to FPGA.

The Video buffer BUF_2 outputs (N2, S2, E2, W2) are fed to COMP_2 (Six comparators) in order to compare the video amplitudes (N2, S2, E2, W2) against each other. The BUF_3 (N2, S2, E2, W2) outputs are driven to a set of 6 comparators for generating N2>S2, E2>W2 and such similar combinations of data. The TTL outputs of the COMP_2 is driven to Level Translators and LV TTL outputs of the Level Translators are fed to FPGA.

2.3. Analog interface section:
- This section consists of ADC’s and Line Receivers.
- The ADC’s are Monolithic 12 bit and 40 MSPS A/D Converter operating at +5V Single Supply and is also compatible with 3V logic.

The Line Receivers/Drivers operate at +5V single supply and are TTL compatible.

The video buffer BUF_4 (N3, E3, S3, W3) outputs are given to two sets of four parallel ADC’s. While each set of ADC’s are operating at different clocks (delayed clocks) derived from the FPGA. N3 is given to two ADC’s, E3 is given to two ADC’s, S3 is given to two ADC’s and W3 is given to two ADC’s. These ADC’s will convert the video input into 12 bit digital data. One set of ADC’s is driven by Clk_B and the other set of ADC’s is driven by Clk_D. Thus 96 bits of digital video amplitude data are given to FPGA.

The PCB has provision for 16 pairs of differential inputs for frequency data and three pairs of differential inputs for controlling data. These bits are received from the VME connector. The total five line receivers are used to convert the differential data to single-ended data. The single-ended data for frequency and controls are given to FPGA through Level Translators.

The frequency data output from the FPGA is taken through Level Translators for converting the differential data to single-ended data. The differential data from the FPGA is taken through Level Translators and routed to the VME connector.

The following outputs are also from the FPGA to the VME connector through Level Translators.
- PSDKC_SP_OUT (4bits), RI_SP_OUT (3bits), SP_OUT (3bits), SW_OUT (4bits), PDW_DATA (36bits), PD_WA_OUT (2bits), PD_PRNS_OUT (1bit), PD_STROBE_OUT (1bit).

The spare inputs and outputs (40 bits) are given to on board Bug Stick connector for monitoring on LSA. The PDW_DATA (36bits), PD_WA_OUT (2bits), PD_PRNS_OUT(1bit), PD_STROBE_OUT(1bit) are also given to Bug Stick connector for monitoring on LSA.

2.4. Memory Interface Section:
- The FLASH MEMORY used in the design is a 256 MBit Flash memory operating at 3.3V.
- The flash memory should have high performance features like:
  o 85 ns initial access
  o 52MHz with zero wait states, 17ns clock-to-data output synchronous-burst read mode
  o 25 ns asynchronous-page read mode
  o 4-, 8-, 16-, and continuous-word burst mode.
  o Buffered Enhanced Factory Programming (BEFP) at 5 μs/byte (Typical)
  o 3.0 V buffered programming at 7 μs/byte (Typical)
3. TESTING

The modules are programmed and interfaced. The interfaced modules are tested individually using Virtex 5 using simulation tool EDK. Flash Memory is tested using Xilinx simulation tool.

The design includes a 24x16 FLASH MEMORY for the purposes of data acquisition. The 24 address lines and 16 data lines are interfaced with FPGA. The control signals are also derived from the FPGA.

And few extraordinary software features like:
- 20 μs (Typical) program suspend
- 20 μs (Typical) erase suspend
- Numony Flash Data Integrator optimized
- Basic Command Set and Extended Command Set compatible
- Common Flash Interface capable

The other peripherals connection is tested using EDK. The other peripherals are connected through Ethernet. Therefore Ethernet is tested in order to check the other peripherals connections. The results in the Figure 3 shows the connection for Ethernet is established.
The Switch Control section is tested with the DIPs and DOPs in Xilinx simulation tool.

Figure 4: Testing output of ADC

Figure 5: Testing output of DAC

Figure 6: Testing output of DIPs
4. CONCLUSION
The analog input Direction Finder and Pulse processor board is implemented based on FPGA. The implemented design is used to find the direction of arrival (DOA) based on Amplitude Comparison Technique involving normalization and calibration of Amplitude data for final computation of DOA. The other functions of this circuit are measurement of pulse parameters like Pulse Width (PW), Pulse Repetition Interval (PRI) & Time of Arrival (TOA) and generation of 32 bit Pulse Descriptor word along with controls. It also generates controls to SP4T (Single –Pole Four Throw) Radio Frequency switch based on maximum signal strength for enabling frequency measurement. The implemented board works for any type of analog signals and is tested for the video signals.

REFERENCES

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