Low Power Test Pattern Generator Using LFSR and Single Input Changing Generator (SICG) for BIST Applications

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ABSTRACT

In this paper we present a comparative power analysis between LFSR and LP-LFSR, where a Low Power test pattern generator using a linear feedback shift register (LFSR), called LP-TPG is presented to reduce the average and peak power of a circuit during testing. The correlation between two test patterns generated by LP-TPG is more than between the random patterns. The main goal of having intermediate patterns is to reduce the transitional activities of primary inputs which reduce the switching activities inside the circuit under test and hence power consumption. An experimental result shows that proposed LP-TPG method gives better result i.e. 30.87% reduction in power as compared to LFSR during testing.

Keywords: built-in self-test, low power, single input pattern testing, switching activity.

1. INTRODUCTION

Complex VLSI testing problems, such as built-in self-test (BIST) technique has been extensively studied and widely used now days. This approach introduces the embedded test structure into the circuit under test (CUT) to make testing easier and better. As we know built-in self-test (BIST), the test patterns are generated and applied to the circuit-under-test (CUT) by on-chip hardware, minimizing hardware overhead which is a major concern of BIST implementation. Unlike stored pattern BIST, which requires high hardware overhead due to memory devices required to store precomputed test patterns, pseudorandom BIST, where as test patterns are generated by pseudorandom pattern generators such as linear feedback shift registers (LFSRs) and cellular automata (CA), requires very little hardware overhead. However, achieving high fault coverage for CUTs that contain many random patterns generated by an LFSR [1]. The linear feedback shift register (LFSR) is commonly used as a test pattern generator (TPG) in low overhead built-in self-test (BIST). This is due to the fact that an LFSR can be built with little area overhead and used not only as a TPG, which provides high fault coverage for a large class of circuits, but also as an output response analyzer. A significant correlation exists between consecutive vectors applied to a circuit during its normal operation. This fact is what has motivated several architectural concepts, such as cache memories, and is central to their effectiveness. This is also true for the high-speed circuits that process digital audio and video signals the inputs to most of whose modules change relatively slowly over time to time. In contrast, the consecutive vectors of a sequence generated by an LFSR are having low correlation. Since the correlation between consecutive vectors applied to a circuit during BIST is significantly lower, the switching activity in the circuit can be significantly higher during BIST than during its normal operation. Excessive switching activity during test can cause several problems. Foremost, since power dissipation in a CMOS circuit is proportional to weighted switching activity, a circuit under test (CUT) can be permanently damaged due to high temperature that is caused by excessive power dissipation if the switching activity in the circuit during test application is much higher than that during its normal operation [2].

However, there are some major drawbacks for this BIST technique whose architecture is based on the linear feedback shift register (LFSR). One is that the BIST circuit introduces more switching activities in the circuit under test during test than that during normal operation [3]. That can cause excessive power dissipation, and results in delay penalty into the design [1]. To lower the power in test mode, many techniques have been proposed to reduce the switching activities of test pattern. For LFSR based test pattern generator (TPG), Guiller proposed a modified clock scheme for linear feedback shift register (LFSR), so that only half of the D flip-flops works during each test period, thus only half of the test pattern can be switched [4]. Single input change sequence technique is a better low power approach which greatly decreases the transitions of inputs to reduce the internal switching activities. In [5], [6], the combination of LFSR and scan shift registers is used to generate random single input change sequences. In [1], a pseudo single input change sequence technique is proposed by adding an extra cyclic shift register and XOR gates, so that a single input change test vectors can be inserted between two neighbour vectors generated by LFSR, n is the length of LFSR. Thus average power is reduced. The drawback of this methodology is that the test vectors’ switching activities will still be very large if the test clock frequency is very high since the seed changes every 2n clock period.

In [7], the combination of LFSR and single input changing generator to generator random single input change sequence. Here the LFSR which is the combination of type-I LFSR and several X-OR gates. Here the main drawback is that the type-I LFSR produces only the correct quotient not the correct remainder for polynomial
In this paper we have taken type-II LFSR which generates more efficient single input change test patterns with single input changing generator (SICG), which includes an n-bit counter and n-bit Grey encoder and 2^n single input changing data are generated. Then the single input changing data is exclusive-ORed with the seed generated by the type-II LFSR. For n-bit LFSR, the largest non-related random data is inserted between two neighbouring seeds, thus 2^n * (2^n-1) single input changing test vectors can be generated. Here the seed generated by the type-II LFSR will be changed every 2^n (m<n=m) clock period, so it was very suitable for BIST in very large scale sequential circuits.

The rest of the paper is organized as follows. Section 2 gives an overview of test of low power analysis. Section 3 presents the proposed design and implementation of LP-TPG architecture. Section 4 describes the experimental results. Section 5 summarizes the concluding remarks.

2. LOW POWER ANALYSIS

There are two major components of power dissipation in a CMOS circuit, one is Static power dissipation due to leakage current or other currents drawn continuously from the power supply and second was Dynamic power dissipation due to charging and discharging of load capacitances and short-circuit current. The following two subsections discuss about the individual power components [9].

2.1 Static Power Dissipation

The static (or steady-state) power dissipation of a circuit is given by the following expression:

\[ P_{\text{STATIC}} = I_{\text{STATIC}} \cdot V_{\text{DD}} \]  \hspace{1cm} (2.1)

where \( I_{\text{STATIC}} \) is the current that flows between the supply rails in the absence of switching activity and \( V_{\text{DD}} \) is the supply voltage. Ideally, the static current of the CMOS inverter is equal to zero, as the positive and negative metal oxide semiconductor (PMOS and NMOS) devices are never ON simultaneously in the steady-state operation. However, there are some leakage currents that cause static power dissipation. The sources of leakage currents are Reverse-Biased pn Junction Leakage Current, Sub-threshold Leakage Current, Gate Leakage Current and Gate-Induced Drain Leakage Current.

2.2 Dynamic Power Dissipation

Dynamic power dissipation mainly depend upon two factors, one is due to Charging and Discharging of Load capacitors and second was due to Short-Circuit Current.

2.2.1 Charging and Discharging of Load Capacitors

For a CMOS inverter, the dynamic power is dissipated mainly due to charging and discharging of the load capacitance. When the input to the inverter is switched to logic state 0, the PMOS is turned ON and the NMOS is turned OFF. This establishes a resistive DC path from power supply rail to the inverter output and the load capacitor \( C_L \) starts charging, where as the inverter output voltage rises from 0 to \( V_{\text{DD}} \). During this charging phase, a certain amount of energy is drawn from the power supply. Part of this energy is dissipated in the PMOS device which acts as a resistor, whereas the remainder is stored on the load capacitor \( C_L \). During the high-to-low transition, the NMOS is turned ON and the PMOS is turned OFF, which establishes a resistive DC path from the inverter output to the Ground rail. During this phase, the capacitor \( C_L \) is discharged, and the stored energy is dissipated in the NMOS transistor. In summary, each switching cycle (consisting of an L to H and H to L transition) takes a fixed amount of energy, which is equal to \( C_L V_{\text{DD}}^2 \). In order to compute the power consumption, we have to take into account how often the device is switched. If the inverter is switched on and off during a given time period, the power consumption is given by,

\[ P_D = C_L \cdot V_{\text{DD}}^2 \cdot f \] \hspace{1cm} (2.2)

where \( f \) represents the number of rising transitions at the inverter output per second.

2.2.2 Short-Circuit Current

Even though under the simplifying assumption of zero rise and fall times for NMOS and PMOS devices for static CMOS logic gates, there exists no direct current path between the power and ground rails, a more realistic timing model for CMOS technology reveals that the input switching is gradual and not abrupt. Consequently, during switching of input, the PMOS and NMOS devices remain ON simultaneously for a finite period. The current associated with this DC current between supply rails is known as short-circuit current \( (I_{\text{SC}}) \). Since short-circuit power is delivered by the voltage supply \( V_{\text{DD}} \), the total power can be written as,

\[ P_{\text{SC}} = I_{\text{SC}} \cdot V_{\text{DD}} \] \hspace{1cm} (2.3)

So the total power consumption of the CMOS inverter is now expressed as the sum of its three components:

\[ P_{\text{TOTAL}} = P_{\text{STATIC}} + P_D + P_{\text{SC}} \] \hspace{1cm} (2.4)

In typical CMOS circuits, the capacitive dissipation was by far the dominant factor. However, with the advent of deep-submicron regime in CMOS technology, the static (or leakage) consumption of power has grown rapidly and account for more than 25% of power consumption in SoCs and 40% of power consumption in high performance logic. So it can be easily found that the power consumption depends on the switching activities for a fixed circuit structure, voltage and fixed clock frequency. The switching activities can be reduced by inserting...
2^n vectors between two neighbouring seeds, in which each vector has only one bit difference with the last vector, thus pseudo random single input changing vectors are generated.

3. DESIGN AND IMPLEMENTATION

As we know LFSR is widely used as test pattern generator because of its small circuit area and excellent random characteristics. Here we used the Type-II LFSR as the seed generator circuit. As shown in Fig 1, the proposed architecture [7] which is called Low Power TPG consists of a seed generator (SG) with type-II LFSR, an n-bit counter, a Gray encoder and an exclusive-OR array. The n-bit counter and Gray encoder generate single input changing patterns.

![Proposed design of Low Power TPG.](image)

According to the design the proposed structure of LP-TPG C[n-1:0] is the counter output and G[n-1:0] is the gray encoder output. The counter and SG are controlled by test clock TCK. The initial value of the n-bit counter is all zeroes, and it generates 2^n continuous binary data periodically. The output of NOR operation of C[m-1:0] will be the clock control signal of SG where m<=n. It can be found that SG will generate the next seed only when C[m-1:0] are all ‘0’ and NOR output changes to ‘1’. The period of the single input changing sequences will be 2^n. Gray encoder in Fig. 1 is used to encode the counters output C[n-1:0] so that two successive values of its output G[n-1:0] will differ in only one bit. Gray encoder can be implemented by following logic.

\[
\begin{align*}
G[0] &= C[0] \oplus C[1] \\
&\vdots \\
G[n-2] &= C[n-2] \oplus C[n-1] \\
G[n-1] &= C[n-1]
\end{align*}
\]

The seed generating circuit SG is a modified LFSR which is the combination of a Type-II LFSR and several XOR gates. The theory in [8] stated that the conventional LFSR’s outputs can’t be taken as the seed directly, because some seeds may share the same vectors. So the seed generator circuit should make sure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. The final test patterns are implemented as following logic.

\[
\begin{align*}
V[0] &= S[0] \oplus G[0] \\
&\vdots \\
V[n-1] &= S[n-1] \oplus G[n-1]
\end{align*}
\]

The Seed Generator’s clock will be TCK/2^m due to the control signal. As SICG’s cyclic sequences are single input changing patterns, the XOR result of the sequences and a certain vector must be a single input changing sequence too. Fig 2 is the circuit structure of single input changing generator (SICG), which consists of an n-bit counter and a Gray code encoder.
The n-bit counter consists of n D flip-flops and the gray encoder consists of n-1 exclusive-OR gates. So the hardware overhead can be controlled under reasonable scope and the power consumption can be greatly reduced while the fault coverage is guaranteed. It is applicable for large scale circuits especially for SoC.

4. EXPERIMENTAL RESULTS

In this section, we present the experimental results of the proposed approach/design. We select the traditional type-II LFSR technique for comparison. Simulation and synthesis which were carried out with Cadence SimVision and Cadence RTL Compiler. Here GPDK 180nm CMOS library was used. In our experimentation we used the polynomial $x^8+x^6+x^5+x+1$ for both type-II LFSR and LP-TPG. The test patterns are generated using an LFSR written in Verilog program. As we used 8-bit LFSR it counts upto $(2^8-1)$ i.e. 255 no. of stages. Fig 3 and 4 shows the behavioral simulation result of 8-bit Type-II LFSR and LP-TPG respectively.
Fig 4 shows the Cadence Simvision output of Low Power Test Pattern Generator (LP-TPG) with test bench used here is parameterized one. As mentioned ‘tck’ and ‘rst’ here is the input of LP-TPG and ‘vout’ represents the output data (8-bits). The results shown in the simvision waveform conforms the theoretical anticipated results. Table 3 shows the comparison of experimental results between type-II LFSR and the test power consumption with the proposed method.

Table 1. Power Consumption Comparison.

<table>
<thead>
<tr>
<th>Circuit/Structure</th>
<th>Dynamic Power(nw)</th>
<th>Total Power(nw)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type-II LFSR</td>
<td>50632.855</td>
<td>50678.282</td>
</tr>
<tr>
<td>LP-TPG</td>
<td>34874.419</td>
<td>35032.540</td>
</tr>
<tr>
<td>IMPROVEMENT (%)</td>
<td>31.12</td>
<td>30.87</td>
</tr>
</tbody>
</table>

In Table 3 the columns refers to the test power consumption with conventional Type-II LFSR circuit and LP-TPG. It can be found that the type-II LFSR circuit consumes 50632.855 nw (50.63 mw) dynamic power and 50687.282 nw (50.67 mw) total test power where as the LP-TPG circuit consumes 34874.419 nw (34.87 mw) dynamic power and 35032.54 nw (35.03 mw) total test power. So there are much more switching activities for multiple input changing sequence while single input changing sequence only change one bit in every clock, thus power consumption is greatly reduced. The result shows that the proposed method can achieve better test power i.e. with 30.87% improvement of power consumption during testing as compared to conventional type-II LFSR.

4. CONCLUSIONS

An efficient low power test pattern generator (LP-TPG) method had been proposed to reduce the test power and uses a modified pseudo-random pattern generator to produce seeds and then operates with the single input changing generator and an exclusive-OR array, thus pseudo-random signal input changing sequences are generated, which greatly minimize circuit switching activities and test power. The experimental result shows 30.87% reduction in test power. LP-TPG also reduces the instantaneous power violation compared to conventional type-II LFSR.

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