Semiconductor-Oxide Interface Properties of Al/Al₂O₃/GaN MOS Capacitor

L. S. YEOH¹, M. J. ABDULLAH², Z. HASSAN³

¹,²,³School of Physics, Universiti Sains Malaysia, 11800 Penang, MALAYSIA.

email: ¹laiseng.yeoh@gmail.com , ²matjohar@usm.my , ³zai@usm.my

ABSTRACT

In this paper, we reported the performance of a Metal-Oxide-Semiconductor (MOS) capacitor fabricated with aluminium oxide (Al₂O₃) dielectric, which was sandwiched between aluminium (Al) gate and n-type gallium nitride (n-GaN) grown on sapphire. This MOS capacitor was characterized using Atomic Force Microscope (AFM), Field Emission Scanning Electron Microscope (FESEM), and Energy Dispersive X-ray (EDX). We acquired a fixed oxide charge density and a mid-gap interface trap density of 8.86 x 10¹⁵ cm⁻² and 3.75 x 10¹² cm⁻² eV⁻¹, respectively. We also investigated the modulation of interface trap density as a function of gate bias.

Keywords: MOS, GaN, Al₂O₃, fixed oxide charge, interface trap

1. INTRODUCTION

MOS is the heart of MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor). MOS forms the basic building block of charge coupled device and it also can be served as storage capacitor in integrated circuits. Although today’s device has been scaled-down into deep submicron regime, silicon (Si) is still widely used as the MOS substrate and it is still dominating about 90% of the semiconductor devices market [1].

Marching into 21st century, semiconductor industry is seeing greater demand on higher power, higher temperature, higher voltage, improved spectra purity, and increased bandwidth, especially in the wireless communication technology. Si is no longer capable to fulfil these ever-increasing demands. Of all design factors, power consumption is the most critical issue as it significantly influences the device reliability. To address this problem, researchers are currently focusing on new semiconductor materials used in power transistor and GaN has emerged as the true contender [2]. This is owing to the unique properties of GaN, such as direct and wide band gap (3.5 eV), large critical electric field (5 MV/cm), high saturation electron drift velocity (2.5 x 10⁷ cm/s), and excellent thermal expansion (5.6 x10⁻⁶ K) [3].

In olden days, GaN film grown on Si substrate was a great interest due to their lower cost and larger size. Nevertheless, large lattice and thermal mismatches between GaN and Si have impeded the GaN-on-Si fabrication process. In recent years, various types of higher quality GaN-based devices have been reported on sapphire substrates, such as p-n junction, p-i-n, p-n-p-n, Schottky, metal-semiconductor-metal, and heterojunction structures [4]. In our study, we used GaN-on-sapphire to fabricate MOS capacitor.

2. EXPERIMENTAL PROCEDURES

A commercially purchased n-GaN grown on C-plane sapphire wafer was used to construct MOS capacitor. A thin Al₂O₃ film with thickness of 80nm was deposited on GaN via radio-frequency sputtering technique. Al was then evaporated onto Al₂O₃ and GaN using a suitable mask to create electrical contacts. The morphology of Al₂O₃ and GaN was analyzed using an AFM and a FESEM, while the compositions of the oxide was determined using an EDX tool. On the other hand, capacitance-voltage (C-V) characteristic and interface trap density of the MOS capacitor were measured using Keithley Instrument with Metrics Interactive Characterization software.

3. RESULTS AND DISCUSSION

3.1 Physical Properties of GaN and Al₂O₃

AFM analysis showed that the as-grown GaN and the as-deposited Al₂O₃ have surface roughness with root mean square (RMS) of 12.81 nm and 8.42 nm, respectively (Fig.1 & Fig.2). FESEM analysis revealed a relatively smooth texture on the GaN surface. On the other hand, formation of isolated bumps with average length of 1.4 μm was observed on the Al₂O₃ surface (Fig.3). EDX analysis proved that the compositions of these bumps were nothing else but Al and O (Fig.4). The formation of bumps could be due to lattice mismatch between GaN and Al₂O₃.

3.2 C-V Characteristic of MOS Capacitor

Fig. 5 depicts the high-frequency (1 MHz) C-V characteristic of the Al/Al₂O₃/n-GaN MOS capacitor with oxide capacitance Cₒₓ of 768 pF, minimum capacitance Cₘᵢₙ of 724 pF, and threshold voltage Vₜ of -2.35 V. The observed high-frequency behaviour was attributed to slow thermally generated minority carriers as a result of large energy band gap in GaN [4]. By using relationship (1) [1], the depletion capacitance Cᵢ was calculated as 12.64 nF.

\[ Cₘᵢₙ = Cₒₓ \times Cᵢ / (Cₒₓ + Cᵢ) \]  

(1)
Fig. 1. (Left) Two dimensional AFM image of surface topography for the as-grown GaN. The observed grain sizes were about 6.6 - 8.8 µm. (Right) Three dimensional AFM image of surface topography for the as-grown GaN. The as-grown GaN had surface roughness with RMS of 12.81 nm.

Fig. 2. (Left) Two dimensional AFM image of surface topography for the as-deposited Al₂O₃. The maximum grain size was 8.9 µm while the minimum was 5.6 µm. (Right) Three dimensional AFM image of surface topography for the as-deposited Al₂O₃. The RMS of surface roughness was 8.42 nm.

Fig. 3. (Left) FESEM micrograph of surface texture for the as-grown GaN (10kx). (Right) FESEM micrograph of the Al₂O₃ surface texture. Distinct islands of averagely 1.4 µm in length were observed on the oxide surface (10kx).

Fig. 4. EDX spectrum of Al₂O₃ deposited on GaN
The relationship between oxide capacitance $C_{ox}$ and oxide thickness $t_{ox}$ with gate area $A$ and oxide permittivity $\varepsilon_{ox}$ is formulized in (2) [1]

$$C_{ox} = \frac{\varepsilon_{ox} A}{t_{ox}}$$

By substituting $C_{ox} = 768 \text{ pF}$, $\varepsilon_{ox} = 9\times8.85 \times 10^{-12} \text{ Fm}^{-1}$, and $A = 7.85 \times 10^{-7} \text{ m}^2$ into (2), $t_{ox}$ of 81.41 nm was obtained. The total capacitance $C$ to oxide capacitance $C_{ox}$ ratio is modelled by (3) [1]

$$\frac{C}{C_{ox}} = \left[1 + \left(\frac{2\varepsilon_{ox} V}{qN_{D}A/t_{ox}^{2}}\right)^{1/2}\right]$$

where $V$ is the gate bias voltage, $q$ is the electronic charge, and $\varepsilon_{s}$ is the semiconductor permittivity. Substrate doping concentration $N_{D}$ of 4.54 $\times 10^{18} \text{ cm}^{-3}$ can be extracted from (3) by using $C = C_{\text{min}} = 724 \text{ pF}$, $C_{ox} = 768 \text{ pF}$, $\varepsilon_{ox} = 9\times8.85 \times 10^{-12} \text{ Fm}^{-1}$, $\varepsilon_{s} = 9.5 \times 8.85 \times 10^{-12} \text{ Fm}^{-1}$, $V = 4 \text{ V}$, $q = 1.60 \times 10^{-19} \text{ C}$, and $t_{ox} = 81.41 \text{ nm}$.

### 3.3. Fixed Oxide Charge

There was no hysteresis loop observed during C-V measurement, reflecting that the effect of mobile ions was negligible. Nevertheless, an obvious flat band voltage shift $\Delta V_{FB}$ was observed along the negative x-axis. This revealed presence of fixed oxide charges $Q_{f}$ in the MOS structure [5]. These near interface oxide charges were considered fixed as they were not influenced by the measurement conditions. In other words, $V_{FB}$ was not affected by the gate voltage sweep rate or the sweep direction [1]. The extrinsic Debye length $\lambda$ is given by [6]

$$\lambda = \sqrt{\varepsilon_{s} kT/q^{2}N_{D}}$$

where $k$ and $T$ are Boltzmann constant and absolute temperature, respectively. With $\varepsilon_{s} = 9.5 \times 8.85 \times 10^{-12} \text{ Fm}^{-1}$, $k = 1.38 \times 10^{-23} \text{ J/K}$, $T = 298 \text{ K}$, $q = 1.60 \times 10^{-19} \text{ C}$, and $N_{D} = 4.54 \times 10^{12} \text{ m}^{-3}$, $\lambda$ was calculated as 1.72 nm. The flat band capacitance $C_{FB}$ is given by [6]

$$C_{FB} = (C_{ox}\varepsilon_{ox}A/\lambda) / (C_{ox} + \varepsilon_{s}A/\lambda)$$

With $A = 7.85 \times 10^{-7} \text{ m}^2$, $\varepsilon_{s} = 9.5 \times 8.85 \times 10^{-12} \text{ Fm}^{-1}$, $\lambda = 1.72 \text{ nm}$, and $C_{ox} = 768 \text{ pF}$, $C_{FB}$ of 753 pF was acquired. The corresponding $V_{FB}$, as extrapolated from Fig. 5, was -1.45 V. The relationship between flat band voltage $V_{FB}$ and fixed oxide charge density $N_{f}$ is given by (6), where $\phi_{min}$ is the difference in work functions between metal ($\phi_{Al} = 4.1 \text{ eV}$) and semiconductor ($\phi_{GaN} = 4.1 \text{ eV}$) [1,6].

$$V_{FB} = \phi_{min} - \frac{q N_{f}}{(C_{ox}/A)}$$

With $V_{FB} = -1.45 \text{ V}$, $\phi_{min} = 0 \text{ V}$, $q = 1.60 \times 10^{-19} \text{ C}$, $C_{ox} = 7.68 \times 10^{-10} \text{ F}$, and $A = 7.85 \times 10^{-7} \text{ m}^2$, $N_{f}$ was found to be $8.86 \times 10^{11} \text{ cm}^{-2}$, which was at the same order as the literature data, such as $6.77 \times 10^{11} \text{ cm}^{-2}$ reported by H. S. Kim et al. in his Al/Ga$_2$O$_3$/p-GaN MOS capacitor [4].

### 3.4. Interface Trap

Our experimental result indicated that the interfacial traps charged and discharged as a function of the gate bias, as illustrated in Fig. 6. Interfacial traps introduced energy levels throughout the band gap at the semiconductor-insulator interface. It may cause distorted or spread-out nature of the C-V characteristic.

![Fig. 6. Interface trap density as a function of gate voltage in the Al/Al$_2$O$_3$/n-GaN MOS capacitor](image-url)
An interface level was assumed to be donor-like in natural. It was positively charged when empty and neutral when filled with an electron. The net charge per unit area of an interface trap \( Q_{it} \) was positive [7].

During accumulation (Fig. 7), the applied gate voltage \( V_G \) placed positive charges on the gate. This caused electrons to be drawn toward the semiconductor-insulator interface and filled most of the interface traps [7]. As a result, the interface trap density \( D_{it} \) approached its minimum value of \( 7.18 \times 10^{13} \) cm\(^{-2}\)eV\(^{-1}\) at +4V (Fig. 6).

During depletion (Fig. 8), the Fermi energy level \( E_F \) lied somewhere at the middle of the band gap at the surface. \( V_G \) placed negative charges on the gate, repelling some electrons away from the semiconductor-insulator interface, and gave rise to \( D_{it} \) [7]. During inversion (Fig. 9), \( E_F \) at the surface was closed to \( E_v \) and all interfacial traps were unfilled by electrons. This was because all energy levels below \( E_F \) were filled with electrons while all energy levels above \( E_F \) were empty (the first order approximation). Thus, \( D_{it} \) reached its maximum value of \( 4.32 \times 10^{14} \) cm\(^{-2}\)eV\(^{-1}\) at -3.61 V during inversion (Fig. 9). In general, \( D_{it} \) (inversion) > \( D_{it} \) (depletion) > \( D_{it} \) (accumulation) [7].

Fig. 7. The condition of the oxide-semiconductor interface during accumulation

Fig. 8. The condition of the oxide-semiconductor interface during depletion

Fig. 9. The condition of the oxide-semiconductor interface during inversion

Interface trap density is plotted against surface potential in Fig. 10 and against interface trap energy in Fig. 11. Interface trap density was constant over the midgap region but it increased abruptly when approaching the band edges. The extrapolated minimum midgap interface trap density \( D_a \) was \( 3.75 \times 10^{12} \) cm\(^{-2}\)eV\(^{-1}\).

4. CONCLUSIONS
The characteristics of Al\(_2\)O\(_3\) as the gate dielectric in an n-GaN based MOS capacitor have been investigated. A low fixed oxide charge density of \( 8.86 \times 10^{11} \) cm\(^{-2}\) and a low mid-gap interface trap density of \( 3.75 \times 10^{12} \) cm\(^{-2}\)eV\(^{-1}\) were achieved, suggesting that it holds promise for use in GaN-based power MOSFET.

REFERENCES