STUDY THE PERFORMANCE ANALYSIS OF LOW POWER–HIGH SPEED CARRY SELECT ADDER USING EDA SIMULATION TOOL

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ABSTRACT

Design of high speed, low power and area-efficient logic circuits is one of the challenging areas of research in VLSI and embedded system design. Adders are the main building blocks in microprocessor as well as DSP processor. Most adders come with the problem of carry propagation delay. To overcome such a problem Carry Select Adder is used as the fundamental computational unit. It is one of the fastest adders. There is scope to reduce power and area in a conventional CSA. This paper deals with different designs of carry select adder, gives a comparative study of such in terms of power, area and delay using gate level (Xilinx) and circuits level (Tanner Spice) simulation tools. Here, five different CSA adders like linear CSA, two stage CSA, three stage CSA, CSA with sharing and SQRT CSA has been analyzed.

Keywords: Carry select adder, CMOS, linear CSA, power, delay, complexity, square root CSA.

I. INTRODUCTION

The design of a Carry Select Adder is such that it operates faster than most conventional adders. The power consumed is such an adder is also moderate and a simple gate level modification is required of a regular CSA to reduce the power. Carry Select Adders are used for high speed application by reducing propagation delay. Though it requires more area than most adders but the design can be implemented in such a way that it can overcome the aforementioned difficulties in the most suitable manner. Building low power VLSI system has emerged as significant performance goal because of the fast technology in mobile communication and computation. The advances in battery technology have not taken place as fast as the advances in electronic devices. So the designers are faced with more constraints; high-speed, high throughput and at the same time consuming as minimal power as possible. They are likely to perpetuate the ability to further reduce the cost per function and improve the performance of integrated circuits. The basic operation Carry Select Adder (CSA) is parallel computation. CSA generates many carriers and partial sum [3]. The final sum and carry are selected by multiplexers. Multiple pairs of Ripple Carry Adders (RCA) are used in CSA structure. Hence, the CSA is not area efficient. The main goal of this Binary to Excess-1 converter (BEC) logic is to use lesser number of logic gate than the n-bit Full Adder. The modified CSA architecture is lower area and power consumption [10–12]. In our project, a parallel study on different types of carry select adder in 4-bit and 8-bit has been presented. They have been compared against various parameters like power, area and speed. Our survey includes: linear CSA, two stage CSA, three stage CSA, CSA with sharing and SQRT CSA. In this paper, we implement the different types of carry select adders and study the performance analysis in terms of power, area and delay using gate level (Xilinx) and circuits level (Tanner Spice) simulation tools.

The rest of the paper is organized as follows: Section II gives a brief description of different types of CSA. Section III deals with the simulation results. Section IV gives the result analysis. Then comes the future work, followed by acknowledgement and conclusion.

II. DIFFERENT TYPES OF CSA

A. LINEAR CARRY SELECT ADDER:

It consists of two ripple carry adders and multiplexers. Addition of two n-bit numbers is done with two ripple carry adders in order to perform calculation twice, one with assumption of carry being zero and other one.

![Fig-1: Block diagram of linear 8 bit CSA](image)

After two results are calculated, the correct sum as well as the correct carry is then selected with the multiplexer once the correct carry is known. Fig.1 shows the block diagram of linear 8 bit carry select adder.
B. TWO STAGE CARRY SELECT ADDER:
The conventional n-bit CSA consists of one \(\frac{n}{2}\)-bit adder for the lower half of the bits and two \(\frac{n}{2}\)-bit adders for the upper half of the bits. Of the two latter adders, one performs the addition with the assumption that \(C_{in}=0\), whereas the other does this with the assumption that \(C_{in}=1\). Using a multiplexer and the value of carry out that is propagated from the adder for the \(\frac{n}{2}\) least significant bits, the correct value of the most significant part of the addition can be selected. Although this technique has the drawback of increasing the area, it speeds up the addition operation [4].

![Fig-2: Block diagram of two stage CSA](image)

C. THREE STAGE CSA:
The idea of iterating the CSA will reduce the delay of the adder. The three stage CSA is given in fig3. For constructing such a \(k\)-bit adder it is divided into \(m\) groups where group \(i\), contains \(P_i\) bits, such that bit width of the least significant part is \(P_1\) and bit width of the most significant part is \(P_m\). In part \(P_m\) adders will be duplicated or there are two adders; one computing addition for carry input 1 and another for carry input 0. Where \(C_{s1}\) is the carry out of \(P_1\) bit adder [4], \(C_{s2}\) is the carry propagated from the other part of adder. \(C_{out}\) is the final carry output of the adder. Similarly we can design for further 4 stage and 5 stage CSA adders to further reduce the delay. The main focus is on value of \(m\). Some effort has been done to improve such adders.

![Fig-3: Block diagram of three stage CSA](image)

D. CSA WITH CHARGE SHARING (CSAS):
Instead of using two separate adders in conventional CSA, one for the \(Cs_1=1\) and another for the \(Cs_1=1\) and another for the \(Cs_1=0\). One adder is used to reduce the area and power consumption. Each of the two additions is performed in one clock cycle. The block diagram of CSAS is shown in fig4. The upper half of the adder i.e. most significant part is 3 bits wide. This part works according to clock. Whenever clock goes high addition for the carry input one is performed. And when clock goes low then carry input is assumed as zero and addition is stored in adder itself. The latch is used to store the sum and carry for \(Cin=1\). Carry out from the previous stage i.e. least significant bit adder is used as control signal for multiplexer to select the final output carry and sum of the adder. If actual carry input is one then for computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. \(C_{out}\) is the output carry [4].

![Fig-4: Block diagram of CSA with charge sharing](image)
E. SQUARE ROOT CARRY SELECT ADDER (SQRT CSA):
Since the speed of a linear CSA is linearly proportional to the bit length \( n \), thus, to optimize the worst-case delay, square root scheme [shown in fig5] will be used in this design of CSA with variable-sized blocks and ripple carry addition in each block [11]. Conventionally, an \( n \) bit square root carry-select adder can be divided into \( p \) stages with sizes \( s_1, s_2 \). Spin an ideal square root scheme, the block size is designed to optimally match the signal arrival time at the final multiplexer input to the delay time of carry-in signal.

III. SIMULATION RESULTS
Input/Outputs waveforms are taken from Xilinx snapshots. Fig.[6-9] are the Input/Output waveforms of different types of CSA.

IV. RESULTS AND ANALYSIS
IV-A: COMPLEXITY ANALYSIS: The area required for operation is calculated by measuring the number of logic gates and the basic adders that have been used by the corresponding circuits. The circuits are counted to the lowest structural level and then the area is calculated [1], [7-8]. The fundamental area specifications that have been allotted to the some basic gates and adders are: All basic gates – 1 unit area, XOR gate – 5 units area, 2:1 MUX – 4 units area, Half-adder – 6 units area, Full adder – 13 units area. The area required by the above mentioned adders are discussed in the table-11.

<table>
<thead>
<tr>
<th>Different CSA</th>
<th>Name of Components</th>
<th>Components Area (Quantity x Area/component)</th>
<th>Total Area (in units)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear CSA</td>
<td>Full adder</td>
<td>16*13=208</td>
<td>248</td>
</tr>
<tr>
<td></td>
<td>2:1 MUX</td>
<td>10*4=40</td>
<td></td>
</tr>
<tr>
<td>Stage2 CSA</td>
<td>Full adder</td>
<td>6*13=78</td>
<td>102</td>
</tr>
<tr>
<td></td>
<td>2:1 MUX</td>
<td>6*4=24</td>
<td></td>
</tr>
<tr>
<td>Stage3 CSA</td>
<td>2:1 MUX</td>
<td>6*4=24</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Ripple carry adder (2-bit)</td>
<td>4*26=104</td>
<td>180</td>
</tr>
</tbody>
</table>

Fig5: Block diagram of 8 bit SQRT CSA

Fig6: Input/output waveform of two stage CSA

Fig7: Input/output waveform of three stage CSA

Fig8: Input/output waveform of three stage CSAS

Fig9: Input/output waveform of SQRT CSA
Table No.2: Delay of different CSA 8bit adder

<table>
<thead>
<tr>
<th>Different CSA</th>
<th>Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear CSA</td>
<td>17.261</td>
</tr>
<tr>
<td>Stage2 CSA</td>
<td>20.026</td>
</tr>
<tr>
<td>Stage3 CSA</td>
<td>16.991</td>
</tr>
<tr>
<td>CSA</td>
<td>14.694</td>
</tr>
<tr>
<td>SQRT CSA</td>
<td>14.613</td>
</tr>
</tbody>
</table>

Fig11: Delay of different CSA 8bit adder

It is apparent that the SQRT carry select adder has the least propagation delay even though it has more area than other adders. Stage2 carry select adder on the other hand has maximum delay but requires the least area. The fig.10 showing the area occupied by the different 8bit CSA adder. The delay of different CSA adders are plotted in fig.11. The SQRT adder uses many different size carry select adders and thus, as a result it requires the largest area.

IV-C: POWER ANALYSIS

Table No.3: Power consumed of different 8bit CSA adder

<table>
<thead>
<tr>
<th>Types of CSA</th>
<th>Avg. Power consumed (in mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear CSA</td>
<td>0.0064</td>
</tr>
<tr>
<td>Stage2 CSA</td>
<td>0.00417</td>
</tr>
<tr>
<td>CSAS</td>
<td>99.3</td>
</tr>
<tr>
<td>SQRT CSA</td>
<td>0.2039</td>
</tr>
</tbody>
</table>
Fig12: Power consumed of different CSA adder

But we can see that the adder with the sharing circuit consumes much more power than any other circuit. The carry select adder with sharing is the most effective one using less area and less time. It is the ideal circuit for addition of data with large number of bits. But it cannot be put into practical use due to its high power requirement. Thus, we can say that the SQRT carry select adder is the more practical and usable one.

CONCLUSION
An estimation of power, delay and area has been made in 8 bit carry select adders. The graphs comparing the power, delay and area of the different carry select adders have been shown in the figures. It is seen from the simulations and the graphs that two stage carry select adder consumes the lowest power whereas the square root carry select adder consumes moderate amount of power and it also has the lowest delay.

REFERENCES