Da-Based DCT with Error-Compensated Adder Tree

CHINABABU PANDURU1, P.MAHESH KUMAR2, C. LEELA MOHAN3
1II M.TECH, 2ASSISTANT PROFESSOR, 3ASSOCIATE PROFESSOR, DEPT OF ECE, CREC, TIRUPATHI.
panduruchinababu@gmail.com, maheshpenubaku@gmail.com, leelamohan416@gmail.com

ABSTRACT

In this paper, by operating the shifting and addition in parallel, an error-compensated adder-tree (ECAT) is proposed to deal with the truncation errors and to achieve low-error and high-throughput discrete cosine transform (DCT) design. Instead of the 12 bits used in previous works, 9-bit distributed arithmetic-precision is chosen for this work so as to meet peak-signal-to-noise-ratio (PSNR) requirements. Thus, an area-efficient DCT core is implemented to achieve 1 Gpels/s throughput rate with gate counts of 22.2 K for the PSNR requirements outlined in the previous works.

Keywords: Distributed arithmetic (DA)-based, error-compensated adder tree (ECAT), 2-D discrete cosine transform (DCT).

1. INTRODUCTION

Discrete cosine transform (DCT) is a widely used tool in image and video compression applications [1]. Recently, the high throughput DCT designs have been adopted to fit the requirements of real-time applications. The high-throughput shift-adder-tree (SAT) and adder-tree (AT), those unroll the number of shifting and addition words in parallel for DA-based computation, were introduced in [3] and [4], respectively. However, a large truncation error occurred. In order to reduce the truncation error effect, several error compensation bias methods have been presented [5]–[7] based on statistical analysis of the relationship between partial products and multiplier-multiplicand. However, the elements of the truncation part outlined in this work are independent so that the previously described compensation methods cannot be applied. This brief addresses a DA-based DCT core with an error-compensated adder-tree (ECAT). The proposed ECAT operates shifting and addition in parallel by unrolling all the words required to be computed. Furthermore, the error-compensated circuit alleviates the truncation error for high accuracy design.

2. MATHEMATICAL DERIVATION OF DISTRIBUTED ARITHMETIC

The inner product is an important tool in digital signal processing applications. It can be written as follows:

\[ Y = A^T X = \sum_{i=1}^{L} A_i X_i \quad \ldots \quad (1) \]

where \( A_i \), \( X_i \), and \( L \) are \( i \)th fixed coefficient, \( i \)th input data, and number of inputs, respectively. Assume that coefficient \( A_i \) is Q-bit two’s complement binary fraction number. The inner product computation in (1) can be implemented by using shifting and adders instead of multipliers. Therefore, low hardware cost can be achieved by using DA-based architecture.

![Fig. 1. Q P-bit words shifting and addition operations in parallel.](image)

3. ECAT ARCHITECTURE

The shifting and addition computation can be written as follows:

\[ Y = \sum_{j=0}^{Q-1} y_j . 2^j \quad \ldots \quad (2) \]

In Fig. 1, the Q P-bit words operate the shifting and addition in parallel by unrolling all computations. Furthermore, the operation in Fig.1 can be divided into two parts: the main part (MP) that includes P most significant bits (MSBs) and the truncation part (TP) that has Q least significant bits (LSBs). Then, the shifting and addition output can be expressed as follows:

\[ Y_{\text{MP}} \quad Y_{\text{TP}} \]
Y = MP + TP · 2^{-(P-2)} \quad \ldots \quad (3)

The proposed ECAT is explained as follows.

A. Proposed Error-Compensated Scheme

From Fig. 1, (3) can be approximated as

\[ Y \approx MP + \sigma \cdot 2^{-(P-2)} \quad \ldots \quad (4) \]

where \( \sigma \) is the compensated bias from the TP to the MP

\[ \sigma = \text{Round}(TP_{\text{major}} + TP_{\text{minor}}) \quad \ldots \quad (5) \]

where \( \text{Round}() \) is rounded to the nearest integer.

The \( \text{TP}_{\text{major}} \) has more weight than \( \text{TP}_{\text{minor}} \) when contributing towards the \( \sigma \). Therefore, the compensated bias \( \sigma \) can be calculated by obtaining \( \text{TP}_{\text{major}} \) and estimating \( \text{TP}_{\text{minor}} \).

B. Performance Simulation for an Error-Compensated Circuit

The \( \varepsilon \), \( \varepsilon_{\text{max}} \), and \( \varepsilon_{\text{mse}} \) are defined as follows:

\[ \varepsilon = \text{Avg} \{|TP - \sigma|\} \quad \ldots \quad (6) \]

\[ \varepsilon_{\text{max}} = \text{max} \{|TP - \sigma|\} \quad \ldots \quad (7) \]

\[ \varepsilon_{\text{mse}} = \text{Avg} \{(TP - \sigma)^2\} \quad \ldots \quad (8) \]

where \( \text{Avg}() \) is the average operator

### TABLE I

<table>
<thead>
<tr>
<th>Error</th>
<th>(P,Q)</th>
<th>(12,3) Case 1</th>
<th>(12,6) Case 3</th>
<th>(12,9) Case 2</th>
<th>(12,12) Case 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \varepsilon )</td>
<td>Direct-T</td>
<td>1.0625</td>
<td>2.5078</td>
<td>4.0010</td>
<td>5.5001</td>
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<tr>
<td></td>
<td>Proposed</td>
<td>0.2656</td>
<td>0.3789</td>
<td>0.3804</td>
<td>0.4738</td>
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<tr>
<td></td>
<td>Post-T</td>
<td>0.2500</td>
<td>0.2500</td>
<td>0.2500</td>
<td>0.2500</td>
</tr>
<tr>
<td>( \varepsilon_{\text{max}} )</td>
<td>Direct-T</td>
<td>2.1250</td>
<td>5.0156</td>
<td>8.0020</td>
<td>11.000</td>
</tr>
<tr>
<td></td>
<td>Proposed</td>
<td>0.6250</td>
<td>1.5000</td>
<td>2.0020</td>
<td>3.0000</td>
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<tr>
<td></td>
<td>Post-T</td>
<td>0.5000</td>
<td>0.5000</td>
<td>0.5000</td>
<td>0.5000</td>
</tr>
<tr>
<td>( \varepsilon_{\text{mse}} )</td>
<td>Direct-T</td>
<td>1.3516</td>
<td>6.7614</td>
<td>16.730</td>
<td>31.224</td>
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<tr>
<td></td>
<td>Proposed</td>
<td>0.1016</td>
<td>0.2184</td>
<td>0.2222</td>
<td>0.3472</td>
</tr>
<tr>
<td></td>
<td>Post-T</td>
<td>0.0859</td>
<td>0.0834</td>
<td>0.0833</td>
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</tbody>
</table>

### TABLE II

<table>
<thead>
<tr>
<th></th>
<th>Shift-add-add</th>
<th>SAT</th>
<th>Proposed ECAT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (gates)</td>
<td>236</td>
<td>406</td>
<td>463</td>
</tr>
<tr>
<td>Delay (ns)</td>
<td>10.8</td>
<td>3.72</td>
<td>3.89</td>
</tr>
<tr>
<td>Area×delay</td>
<td>100%</td>
<td>59.3%</td>
<td>70.7%</td>
</tr>
<tr>
<td>( \varepsilon_{\text{mse}} )</td>
<td>0.326</td>
<td>6.761</td>
<td>0.218</td>
</tr>
</tbody>
</table>

C. Proposed ECAT Architecture

The proposed ECAT has the highest accuracy with a moderate area-delay product. The shift-and-add [2] method has the smallest area, but the overall computation time is equal to 10.8(=1.8x6) ns that is the longest. Similarly, the SAT[10], which truncates the TP and computes in parallel, takes 3.72 ns to complete the computation and uses 406 gates, which is the best area-delay product performance. However, for system accuracy, the SAT is the worst option shown in Table II. Therefore, the ECAT is suitable for high-speed and low-error applications.
4. PROPOSED 8 × 8 2-D DCT CORE DESIGN

The 1-D DCT employs the DA-based architecture and the proposed ECAT to achieve a high-speed, small area, and low-error design. The 1-D 8-point DCT can be expressed as follows:

\[ Z_n = (\frac{1}{2})k_0 \sum_{m=0}^{7} x_m \cos((2m+1)n\pi/16) \] ………..(9)

Where \( x_m \) denotes the input data; \( Z_n \) denotes the transform output; the proposed 2-D DCT is designed using two 1-D DCT cores and one transpose buffer. For accuracy, the DA-precision and transpose buffer word lengths are chosen to be 9 bits and 12 bits, respectively, meaning that the system can meet the PSNR requirements outlined in previous works. Moreover, the 2-D DCT core accepts 9-bit image input and 12-bit output precision.

5. DISCUSSION AND COMPARISONS

Table IV compares the proposed 8 × 8 2-D DCT core with previous 2-D DCT cores. In [3] and [4], the SAT and AT architectures for DA-based DCTs improve the throughput rate of the NEDA method. However, DA-precision must be chosen as 13 bits to meet the system accuracy with more area overhead. The proposed DCT core uses low-error ECAT to achieve a high-speed design, and the DA-precision can be chosen as 9 bits to meet the PSNR requirements for reducing hardware costs. The proposed DCT core has the highest hardware efficiency, defined as follows (based on the accuracy required by the presented standards)

\[ \text{Hardware Efficiency} = \frac{\text{Throughput Rate}}{\text{GateCounts}} \] …….. (10)

**TABLE III**

| COMPARISONS OF DIFFERENT 2-D DCT ARCHITECTURES WITH THE PROPOSED ARCHITECTURE |
|-----------------------------------------------|-------------------------------|----------------|
| Technology                                | NEDA                          | DA-based        | DA-based |
| Multipliers/ROMs                          | 0/0                           | 0/0             | 0/0      |
| Adders                                    | 92                            | 50+16AT         | 46+16 ECAT |
| DA-precision                              | 12 bits                       | 13 bits         | 9 bits   |
| Throughput Rate(pels/sec)                 | 77M†                          | 400 M           | 1G       |
| Hardware Efficiency                       | 3.42                          | 10.05           | 45       |

†77MHz=1GHz/13

6. CONCLUSION

In this brief, a high-speed and low-error 8 × 8 2-D DCT design with ECAT is proposed to improve the throughput rate significantly up to about 13 folds at high compression rates by operating the shifting and addition in parallel. Furthermore, the proposed error-compensated circuit alleviates the truncation error in
In this way, the DA-precision can be chosen as 9 bits instead of 12 bits so as to meet the PSNR requirements. Thus, the proposed DCT core has the highest hardware efficiency than those in previous works for the same PSNR requirements. Finally, an area-efficient 2-D DCT core is implemented using a TSMC 0.18-
_m process, and the maximum throughput rate is 1 Gpels/s. In summary, the proposed architecture is suitable for high compression rate applications in VLSI designs.

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REFERENCES