CMOS Digital-Phase-Locked-Loop for 1 Gbit/s Clock Recovery Circuit

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ABSTRACT

The proposed DPLL for 1GHz clock recovery application has been designed and simulated using LT spice 50nm CMOS process. Two simulations, one with alternate strings of ones and zeros and another with strings of seven zeros followed by one (NRZ encoding scheme), have been performed without using initial conditions to the loop filters and other using the initial conditions. It is found that there is a trade-off between lock time, loop filter capacitor, initial conditions to the loop filter, gain of the VCO and ripples on the output of the VCO.

Keywords: Hogge PD, Charge-pump, loop filter, input voltage to the VCO and VCO gain

1. INTRODUCTION

The digital phase-locked loop, DPLL, is a closed loop frequency system that locks the phase of an output signal to an input reference signal. It is a circuit that is used frequently in modern integrated circuit design. DPLL’s are widely used in computer, radio, and telecommunications systems where it is necessary to stabilize a generated signal or to detect signals. The term “lock” refers to a constant or zero phase difference between two signals [1].

Basically, data transmitted should be processed and recovered as it is at the receiver end. However, practically, the data is distorted when processed at the receiver end due to nonlinearities at the receiver amplifier and the finite communication channel-bandwidth and absence of a clock makes it difficult to recover the transmitted data. Encoding the digital data so that the duty cycle of the resulting encoded data is 50% helps in preventing nonlinearities (distortion) in the input data of the receiver and increases the channel bandwidth for a constant data rate. And a circuit that generates a clock signal which is locked or synchronized with the incoming signal is required so that the transmitted data are recovered in the original format at the receiver end. This application of DPLL is often termed as clock-recovery circuit or bit synchronization circuit [1].

The DPLL, generally, consists of the phase detector (PD), the charge pump, loop filter and voltage-controlled oscillator (VCO). The details of each of these blocks are discussed below:

2. PHASE DETECTOR (PD)

There are two types of phase detector namely XOR phase detector and Phase Frequency detector (PFD). The design requirements of the VCO used with PFD is much more relaxed than those of XOR phase detector. So, it is mostly preferred than XOR PD. There is also another type of phase detector called Hogge phase detector which operates in a similar way like the phase frequency detector except it is self correcting and independent of the data rate, the temperature or process variations. Instead of UP and DOWN in PFD, the outputs are named as “Increase” and “Decrease”. So, this phase detector is used in this design. Fig.1. is the basic block diagram of Hogge PD.

Nodes A and B are simply the input NRZ data shifted in time by one-half bit-interval and one bit-interval, respectively. If “Increase” is low more often than “Decrease”, the average voltage out of the loop filter and thus the frequency out of the VCO will decrease and vice-versa.

![Fig.1. Hogge phase detector](image1)

![Fig.2. Simulation of the Hogge PD](image2)
The above simulation shows that the width of the increase signal is wider compared to the decrease signal. In order to avoid these, a delay is added to the XOR gate of the increase signal. After adding delay, the simulation result shows that the width of the increase and decrease signals is almost similar.

The equation of phase is given as \( \Delta \phi = \frac{\Delta t}{T_{\text{clock}}} \cdot 2\pi \) (radians)

Where \( \Delta t \) is the phase difference between the rising edges of increase and decrease signal and \( T_{\text{clock}} \) is the time between the edges of the clock. The phase difference, \( \Delta \phi \), is zero when the loop is in lock.

Fig. 3. Adding a delay to compensate the increase signal  
Fig. 4. Simulation result of Hogge PD after adding delay

3. CHARGE-PUMP OUTPUT AND LOOP FILTER

Since there are two outputs from the PD, it should be combined into a single output to drive the loop filter. There are two methods of combining: tri-state output and charge-pump output. Since the current source in charge-pump can be made insensitive to the variation in VDD, modulation of the VCO control voltage \( V_{\text{inVCO}} \) is absent. So, charge-pump output is preferred over the tri-state.

The output current of the charge-pump can be written as, \( I_{PD} = K_{PD} \cdot \Delta \phi \)  

where \( K_{PD} = \frac{i_{\text{pump}}}{2\pi} \) (amps/radian).

The charge-pump loop-filter transfer characteristic is given by

\[
V_{\text{inVCO}} = I_{PD} \cdot \frac{1}{j\omega (C_1 + C_2)} \cdot \left[ 1 + \frac{R}{C_1 + C_2} \right] = K_F \cdot I_{PD} 
\]  

The loop filter integrates the charge supplied by the charge-pump. The capacitor \( C_2 \) prevents \( I_{pump} \cdot R \) from causing voltage jumps on the input of the VCO and thus frequency jumps in the DPLL.

The loop filter transfer function (neglecting \( C_2 \) since it is set one-tenth of \( C_1 \) generally) is given by, \( K_F = \frac{1 + \frac{R}{C_1}}{s C_1} \)  

The feedback loop transfer function is given by

\[
H(s) = \frac{K_{PD}K_{VCO}(1+sR)}{s^2 + \left( \frac{K_{PD}K_{VCO}}{C_1N} \right) s + \frac{K_{PD}K_{VCO}}{N C_1}}
\]

The natural frequency from the transfer function is given by

\[
\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N C_1}}
\]

and the damping factor is given by \( \zeta = \frac{\omega_n}{2} \cdot RC \)
4. VOLTAGE CONTROLLED OSCILLATOR (VCO)

There are two types of VCO: Current-starved VCO and Source coupled VCO. Since the later requires a capacitor which may not be available in a single-poly pure digital process without using parasitic and there is a reduce output voltage swing, current-starved VCO is more preferred.

In this paper, a fully differential VCO is used. Using any number of stages, a fully differential VCO can be implemented with the delay elements and proper feedback while using an even number with the inverting (non-inverting) output fed back and connected to the non-inverting (inverting) input to generate input in-phase and quadrature signals.

Eight stages fully differential VCO is used in this paper and the figure is shown below:

![Fig. 6. 8 stage VCO](image)

Since the logic levels are not high at the outputs, it is necessary to regenerate full logic levels without introducing skew into the output. Figure below is the modified 8 stage VCO where the 8th stage is changed to two differential-amplifier with swapped input signals so that a positive and minus outputs can be generated and two inverters are added at the two outputs to provide delay so that a full logic level is obtained.

![Fig. 7. Simulation result of 8 stage VCO](image)

![Fig. 8. Modified 8 stage VCO](image)
In this paper, VCO is assumed to oscillate at 1 GHz when $V_{\text{invVCO}}$ is approximately 350 mV (which is not $V_{DD}/2$). Since Hogge PD doesn’t perform frequency detection (like PFD) care must be taken with locking on harmonics. So, initial conditions on the loop filter need to be used to set the initial clock frequency close to correct values to avoid locking on harmonics. For one complete oscillation of the VCO, the signal must travel through the VCO twice.

The gain of the VCO is given as,

$$K_{\text{VCO}} = \frac{2\pi}{T_{\text{max}} - T_{\text{min}}} = \frac{2\pi}{11 \times 10^9\text{ radian/s}} = \frac{2\pi}{11 \times 10^9\text{ radian/V.s}}$$

where assumption is made that at 350 mV the output frequency is 1 GHz. If $V_{\text{invVCO}}$ is increased by 100 mV, the period is decreased by approximately 150 ps, resulting in an output frequency of 1.175 GHz (period is 850 ps approximately).

When Hogge PD is used with the charge-pump, the gain is given by

$$K_D = \frac{I_{\text{pump}}}{\pi}$$

By setting $I_{\text{pump}} = 10\mu A$, $K_D = 3.2 \mu A/\text{radian}$.

Setting the natural frequency $\omega_n = 100 \times 10^6 \text{ radians/s}$ and $\zeta = 1$ and substituting in eqn. (vi), $R C_1 = 20\text{ns}$ and using eqn. (v) and $N=1$, $C_4 = \frac{K_D K_{\text{VCO}}}{\omega_n^2} = 3.5 \text{ pF}$

Set $C_1 = 3.5 \text{ pF}$, $R = 5k$ and $C_2 = 0.35pF$ (one-tenth of $C_2$) in the final block diagram of DPLL clock-recovery circuit as shown below:
In the first simulation, an alternating string of ones and zeros is applied. Since the data rate is 1 Gbit/s, the width of a one or a zero is 1 ns. No initial condition is applied to the loop filter. However, because the NRZ data is full of transitions, $V_{\text{inVCO}}$ quickly moves to around 350 mV. The lock time depends on the input data.

For the second simulation, the voltage across the loop filter, $V_{\text{inVCO}}$, is initialized at 340 mV (slightly below the final of around 340 mV). After approximately 600 ns, the loop locks. If it is not initialized, the lock time and the simulation time required to attain lock is quite long. Since the gain of VCO is large, not initializing $V_{\text{inVCO}}$ results in VCO oscillating at the wrong frequency and the loop locking incorrectly when the data is an alternating string of ones and zeros or some other pattern. To avoid this, the practical solution is reducing the gain of VCO.
CONCLUSION
The proposed DPLL for 1GHz clock recovery application has been designed and illustrated. Two simulations, one with alternate strings of ones and zeros and another with strings of seven zeros followed by one (NRZ encoding scheme), have been performed without using initial conditions to the loop filters and other using the initial conditions. It is found that there is a trade-off between lock time, loop filter capacitor, initial conditions to the loop filter and ripples on the output of the VCO.

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