Lay out Design of 4-bit Ripple Carry Adder Using NOR and NAND Logic

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ABSTRACT
A fine deal of creativeness can be exercised and a huge amount of time wasted exploring layout to minimize the size of a gate or other circuitry such as an adder or memory element in an integrated circuit. This paper represents a clear-cut and power calculations for 4-bit Ripple Carry adder using NAND and NOR gates. Layout design for 4-bit Ripple Carry adder using only CMOS NOR gates and CMOS NAND gates with the help of Micro wind as a tool for design and simulation. The performance parameters are analyzed from the simulation responses and Calculated the Power Consumption.

Keywords: Layout, Ripple Adder, Simulation.

[1]. INTRODUCTION
The trend of CMOS (Complementary Symmetry Metal Oxide Semiconductor) technology improvement continues to be driven by the need to integrate more functions within a given silicon area, reduce the fabrication cost, increase operating speed and dissipate less power. Past few years industrial production of high performance integrated circuits IC). [1] Two important characteristics of CMOS devices are high noise immunity and low static power consumption Significant power is only drawn when the transistors in the CMOS device are switching between on and off States. Consequently, CMOS devices do not produce as much transistor logic (TTL) or NMOS logic. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

Micro wind is a CMOS circuit editor and simulation tool for logic and layout-level design, running on Microsoft Windows. It has been developed since 1998 through several versions, and is available as a freeware (Lite version [6]) for educational purpose. In this paper, a 4-bit binary parallel adder based on CMOS NAND and NOR gate layout’s are designed using Micro-wind 2.7. First of all the individual components, the NAND inverter, 2-input, 3-input and 4-input NAND gates were designed, aligned and connected properly. The overall the previous adder. This kind of adder is ripple carry adder, since each carry bit “ripples” to the next full adder.

[2]. BACKGROUND THEORY
A and B respectively and $C_{n-1}$ is the carry generated from the addition of $(n-1)$th order bits. Table 1 shows the truth table and figure 1 shows the logic diagram of a 1-bit full adder. Logical circuit using multiple full adders to add N-bit numbers can be created. Each full adder inputs a $C_{in}$ which is the $C_{out}$ of

<table>
<thead>
<tr>
<th>Input bit number</th>
<th>Input bit number</th>
<th>Carry bit input</th>
<th>Sum bit output</th>
<th>Carry bit output</th>
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<tbody>
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</table>

Fig 1. 1-bit Full adder

[3]. DESIGN OF THE RIPPLE CARRY ADDER
A ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascaded with the carry output from each full adder connected to the carry input of the next full adder in the chain. Fig 2. shows the interconnection of four full adder (FA) circuits to
provide a 4-bit ripple carry adder. Notice from Fig 2. that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits $a_0$ and $b_0$ in the figure represent the least significant bits of the numbers to be added. The sum output is represented by the bits $s_3$.

![Fig 2. 4-bit Ripple Carry Adder](image)

**[4].REALIZATION OF A CMOS NOR ADDER:**

![Fig 3. Full adder using NOR gates.](image)

Fig 4 shows the 4-bit Ripple adder to obtain the sum and carry using NOR gates.

![Fig 4. 4-Bit Ripple Carry Adder Using NOR gates.](image)

Fig 5 shows the Layout of 4-Bit Ripple Carry Adder Using NOR gates obtained for 120nm Technology by compiling Verilog file generated from Digital schematic software.

![Fig 5. Layout of 4-Bit Ripple Carry Adder Using NOR gates](image)

**[5].REALIZATION OF A CMOS NAND ADDER**

Here proposing the adder circuit using NAND gates for sum and carry as shown in the figure.
While in NAND devices an erase operation is not straightforward, NOR does require all bytes in the block to be written with “zeros” before they can be erased. Since the size of erase blocks in NOR devices ranges from 64Kbyte to 128Kbytes (in NAND: 8Kbytes to 32Kbytes), such a write/erase operation can take up to 5 seconds(!). In stark contrast, NAND performs the identical operation in 4 msec maximum. The erase block size difference further increases the performance gap between NOR and NAND, as statistically more erase operations must be performed in NOR-based units per any given set of write operations (especially when updating small files).

![Fig 6. NAND realization of $S_n$ and $C_n$ for binary Adder.](image)

![Fig 7. 4-Bit Ripple Carry Adder Using NAND gates.](image)

Fig 6 shows the 4-bit Ripple adder to obtain the sum and carry using NAND gates.

**Performance Comparison between NAND Adder and NOR Adder:** CMOS logic dissipates less power than any other logic circuits. This is because CMOS dissipates power only switching (“dynamic power”). Here we are proposing the Power Consumption of 4-bit NAND Adder and 4-bit NOR Adder as shown in below.

![Fig 7. 4-Bit Ripple Carry Adder Using NAND gates.](image)

![Fig 8. Layout of 4-Bit Ripple Carry Adder Using NOR gates is obtained for 120nm Technology by compiling Verilog file generated from Digital schematic software.](image)

Fig 8. Shows the Layout of 4-Bit Ripple Carry Adder Using NOR gates is obtained for 120nm Technology by compiling Verilog file generated from Digital schematic software.

![Fig 8. Layout of 4-Bit Ripple Carry Adder Using NOR gates](image)

![Fig 9. Simulation Result of NAND adder](image)

![Fig 10. Simulation Result of NOR Adder](image)
CONCLUSION:
This paper presents a basic and compact formation of a 4–bit Ripple Carry Adder using NAND and NOR gates. The 4-bit ripple carry adder is chosen for implementation as it supports detailed analysis, clear design topology and ease of verification. It is designed using basic approach, gate level approach, and universal gate level approach. For modular structures, NAND gate based design proved more efficient than NOR gate based design. Also from the Comparison of the Power Consumption of these designs for adders, NAND and NAND-based solutions are ideal for high capacity data storage, while NOR approach is best suited for code storage and execution, usually in small capacities.

![Comparison Graph]

Fig.11 .Comparison Graph

REFERENCES:

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