Vol 05, Article 10468, October 2014 International Journal of VLSI and Embedded Systems-IJVES
http://ijves.com ISSN: 2249 – 6556

BUILT-IN GENERATION OF FUNCTIONAL BROADSIDE TEST FOR ISCAS-85 C432

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ABSTRACT

In this proposed method we are test the one combinational circuit. Here this combinational circuit having 36-bit input and 7-bit output. ISCAS-85 C432 27-channel interrupt controller is a combinational benchmark circuit. In this paper describes that an on-chip test production technique of functional broadside test. The hardware was based on the request of principal input sequences original from a known reachable state, thus using the circuit to manufacture additional reachable states. Random primary input sequence was changed to remove the repetitive synchronization and thus yield varied set of reachable states. The hardware arrangement was simple and fixed, and it was modified to a given circuit only from side to side the following parameters: the measurement lengthwise of the LFSR used for generating a accidental primary input sequence; the length of the main input sequence; the specific gates used for modifying the accidental primary input sequence; the exacting gate used for selecting practical tests; and the seeds for the LFSR. With the planned on-chip test generation technique, the circuit is used for generate available states for the period of test application. This alleviates they would like to calculate available states offline.

KEY WORDS: *Built-in test generation, functional broadside tests, ROM,, reachable states, transition faults, test pattern generator,ISCAS-85 C432 benchmark circuit.*

1. INTRODUCTION

Built In Self Test (BIST) is considered the best solution for testing the circuit itself i.e. the testing blocks are included with in the circuit. For the purpose of testing additional three hardware blocks are required to digital circuit.

1. Test pattern generator
2. Response analyzer
3. Test controller

Test pattern generator gives the test patterns to the Circuit under Test (CUT) different types of test pattern generators are Linear Feedback Shift Register (LFSR), counter, and ROM with stored patterns. A response analyzer is a comparator with stored response it compacts and analyzes the test response and checks the exactness of CUT. In the response analyzer test response compression techniques are used these are one's count, transition count ,parity checker and signature analysis. The test controller block is used to active the testing and analyzing the responses. In general, by using test controller circuit, test related functions can be executed.

The Fig.1 shows that, the primary inputs to the MUX and the primary outputs from the CUT cannot exist in the process of testing BIST operation. The inputs to the CUT are received from other modules so that it can perform the function to meet its designed purpose during general operation. While performing test mode, the examination pattern sequence are applied by the hardware pattern generator to the CUT through MUX and the evolution of response of the test done by an output response comparator. In the most common type of BIST, the test response stored in the output response compactor. The generated signatures (response signatures) compared with the reference signatures (golden signatures) stored in the ROM.

Mainly four parameters have to be taken in the increasing methodology of BIST for the Hardware systems design ; these parameters correspond by

The means of design parameters for the design techniques of the system discussed.

1. Fault coverage: It is the percentage of faults detected during the test process, the test pattern generator generates the patterns and detected by the output response observer. In the manufacturing test, it is required that high fault coverage. In some cases there is a error in the bit stream generated in the response signatures matches with the golden signatures and the test results shows that hardware is fault free, this is unwanted propriety is called aliasing or masking.
2. Size of test set: It is the total numbers of test patterns twisted by the hardware test generator, and is personally linked to fault coverage: generally, for the covering of high fault coverage it requires large size of test set.
3. Hardware over head: In some cases the requirement of more hardware for the design of BIST is called overhead. In the most of hardware systems design, high amount of hardware is inacceptable.

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4. Performance overhead: In the design of hardware system it is more significant than that of hardware overhead. It is mainly depend up on the numbers of critical path (worst-case) delays present in the hardware system. For the best hardware system requires less numbers of critical path delays.

2. BLOCK DIAGRAM OF BIST

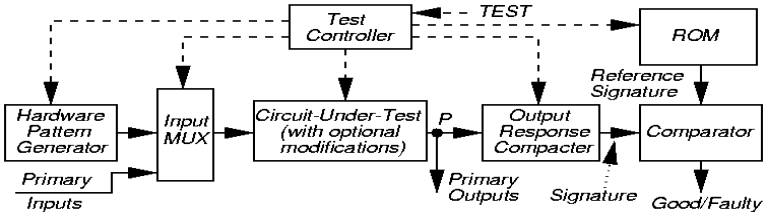

Fig.1 Block diagram of BIST

The advantages of BIST are fast, efficient and hierarchical, same hardware is capable of testing chips, boards and systems. Built in Self Test can be used in two modes one is on-line mode and other one is off-line mode. In the on-line mode again two types these are concurrent, in this simultaneous operation with normal operation; next one is non-concurrent in this test done when the system is in idle. In the off-lone mode (function is suspended) in this two methods are present depending on functioning of CUT and depending on structure of CUT.

The On-line BIST mode is generally implements with two goals these are covering of faults and small fault latency, So for this test pattern generator (TPG) and output response analyzer (ORA) are normally designed for the covering of guarantee fault models, less hardware overhead and satisfactory of number of set size. Different techniques are used in different parts of the system to meet the above goals.

Generally LFSR (linear Feed Back Shift Register) is used for the implementation of TPG and ORA.LFSR is like a shift register made up of some standard flip-flops, from the selected flip-flops takes the output and connected back to the inputs of shift register. In the design of TPG, the LFSR set repeats rapidly through more number of states. The number of states depends on the design parameters and test patterns of LFSR. For the TPG (Test Pattern Generator) different techniques are used but in this paper we are using pseudo random tests. In the pseudo random test the LFSR produces the test patterns with equal number of 0's and 1's on each input line. In the tests biased distribution of 0's and 1's captures more faults and less number of test vectors. For the using of ORA (Output Response Analyzer), the LFSR counts the responses generated by the tests. An LFSR ORA finally stores the sequence of test responses in the form of signatures, after that it can be compared with the reference signature for the observation of fault is present or not. In the Random BIST method, make sure that high fault coverage, and sufficiently less number of tests. For the decreasing of cost of the LFSR's the generated test sequence must be shorter .In the hardware design for improving of controllability and observability the test points can be inserted in the CUT. Because of less number of test sequence and inserting of test points the performance is poor. To improve the performance, in the generated test sequence, inserting a specific "seed" tests that are known to detecting the hardware faults.

Fig.2 shows that standard LFSR circuit used in the BIST. The Linear Feedback Shift Register (LFSR) circuits are mainly two types

1. Internal type
2. External type

In this paper external type is used. The output patterns of the LFSR are shifted by time and sequentially they become correlated, from the above process effectiveness of the fault detection is reduced. Hence a phase shifter (connected with XOR gates) is often used the output patterns of LFSR which is de-related. To find out whether the CUT is faulty or not, the response of CUT is compacted by MISR (Multiple Input Shift Register) to a small signatures and these signatures send to comparator, which compares with the reference signatures.

Pseudo-Random Pattern Generation

A pseudo-Random Pattern Generation is a string of one's and zero's .In this generation the bits are appeared to be random, but sometimes the generation will be repeatable in the generation the LFSR is commonly used. In normal pseudo-random pattern generation requires less patterns than that Exhaustive test but more patterns than deterministic ATPG. In comparing with the other method the pseudo random pattern generator requires high test time and necessitates evolution of fault coverage by using fault simulation. In this type pattern it has potential for less hardware, less performance overhead and less design effort than the other methods .In this method each bit has an approximately equal probability of one's and zero's and quantity of a pattern is applied typically in the order of 10^3 to 10^7 in this pattern the fault coverage and circuit testability is required.

The BIST technique based on control of LFSR state the linear feedback shift register reseeding is one of the examples. LFSR reseeding may be static or dynamic. In the static condition, the LFSR stops the pattern

Vol 05, Article 10468, October 2014 International Journal of VLSI and Embedded Systems-IJVES
http://ijves.com ISSN: 2249 – 6556

generation while taking seeds, but in the dynamic condition simultaneously process taken place loading the seeds as well as pattern generation .The seed length is less than the LFSR (partial reseeding) or equal to the size of LFSR (full reseeding) for the encoding test vector partial reseeding is introduced which allows the dynamic reseeding technique. The solution of linear equations obtains the seeds and test vectors are arranged to provide with a group of linear equations.

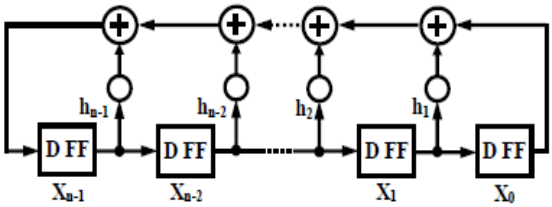

Fig.2 Standard LFSR circuit

C432 COMBINATIONAL BENCHMARK CIRCUIT

In many industries the standard benchmark circuits are used they will be like ISCAS-85 , ISCAS-89 etc are used. The ISCAS-85 represents the combinational circuits and ISCAS-89 represents the sequential circuits. These benchmark circuits are used to examine the latest hardware design and testing of manufacturing approaches and different technologies. A detailed explanation of one of the ISCAS-85 benchmark circuit is C432 interrupt controller.

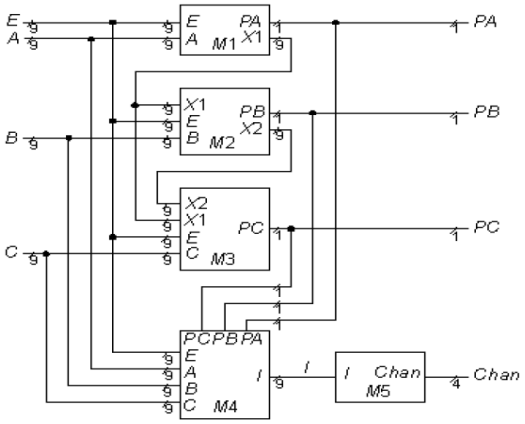

Fig. 3 C432 Combinational Circuit

Fig.3 shows that combinational circuit of C432. The C432 having 27- channel interrupt controller .The input channels are divided into three buses each having 9 bits in it. These three buses are A, B and C. Additional 9 bit bus (E) which is used for enabling and disabling of interrupt requests the bit positions.
In the C432 the number of logic gates are used at the primary input is (2^36).
The C432 having 36 inputs, 7 outputs and 160 gates.

Function of C432: The bit positions inside the each bus determines the priority of interrupt request among three 9 bit buses ,these are represented as A,B, and C. The additional 9 bit bus is known as 'E' is used for enabling and disabling of interrupt requested. In Fig.3 shows that each module are named as M1, M2, M3, M4 and M5 in each module underling logic present.

Test Generation Strategies Comparison:

In the test pattern generation the design effort, hardware overhead, fault coverage and test time overhead are the main issues in the implementation of BIST strategy. The table 1 shows that comparison of different test strategies.

Table 1 Comparison of different test strategies

Test Generation Methodology	*Fault Coverage*	*Hardware Overhead*	*Test Time Overhead*	*Design Effort*
Stored Pattern	High	High	Short	Large
Exhaustive	High	Low	Long	Small
Pseudo-exhaustive	High	High	Medium	Large
Pseudo-random	Low	Low	Long	Small
Weighted Pseudo-random	Medium	Medium	Long	Medium

Vol 05, Article 10468, October 2014
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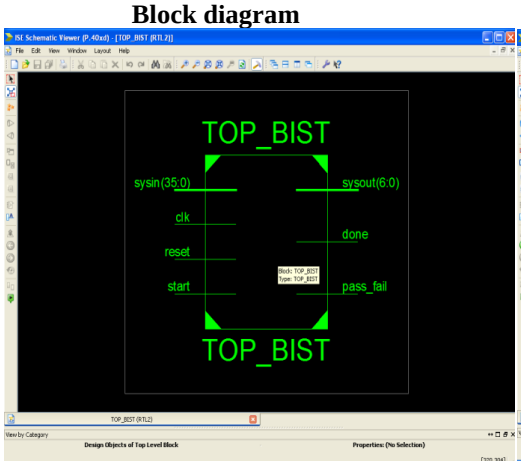
Compression/Compaction of BIST Response Techniques

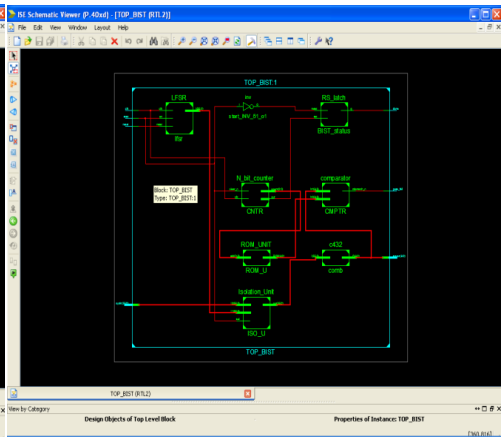
While performing the BIST operation, the output response analyzer (ORA) is takes the more amount of data from CUT responses .Suppose in the circuit we are taken 200 outputs and we are interested in generating 5 million random patterns in this case the CUT response to ORA will be 1 million bits, So in practice this is not manageable hence it is essential to compress this large amount of circuit responses to a manageable size that can be stored in the chip. The ORA is compresses the high test response in to a single word this word is called a signature (response signature) this signature is then compared with the golden signature which is stored in ROM the golden signature is a fault-free response using the same compression technique if the response signature matches with the golden signature the CUT is fault-free otherwise faulty. The different types of response analysis methods are signature analysis, syndrome count, ones count and transition count.

3. RESULT ANALYIS

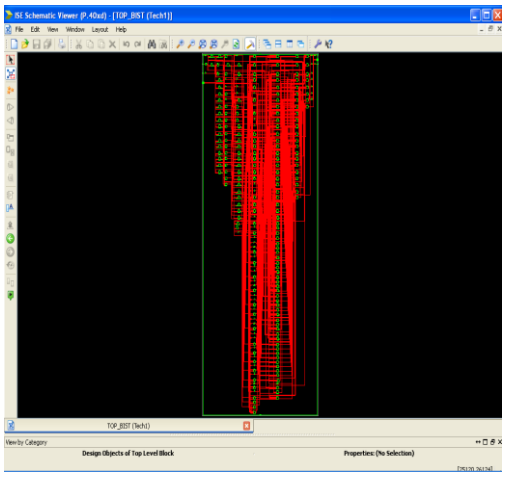
Block diagram



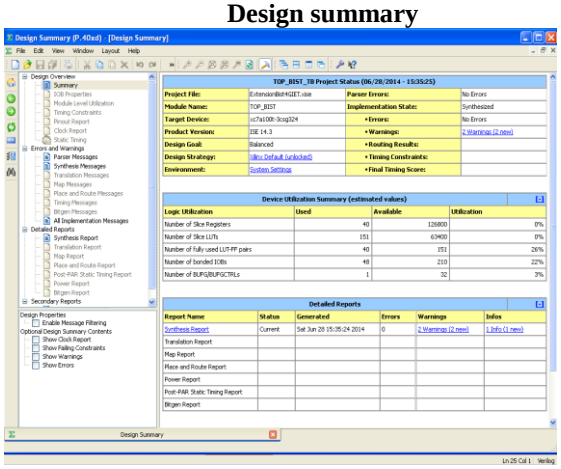
RTL schematic



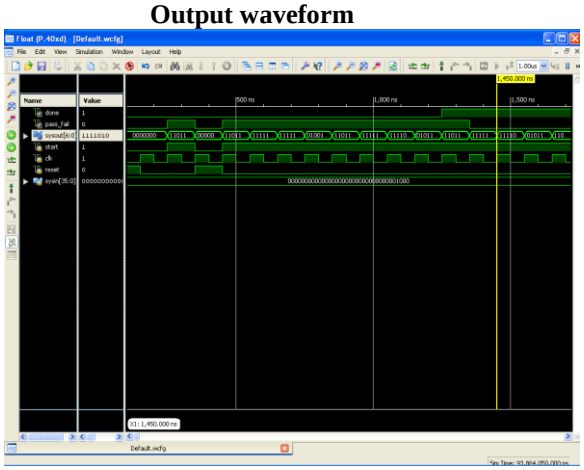
Technology schematic diagram



Design summary



Output waveform



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http://ijves.com ISSN: 2249 – 6556

4 .CONCLUSION

The propose method implemented to test one of the combinational circuit by using Built in self test circuit. The presence of delay-inducing defects is causing increasing concern in the semiconductor industry nowadays. To test used for such delay-inducing defects, scan-based transition responsibility testing techniques are being implemented. To Full scanning Process resolve Generated and then Fault coverage for Broadside testing is 80%, functional broadside testing is 40% and pseudorandom testing is 80%. Maximum length of testing full scan circuit is 402. Scanning percentage is 97%. Testing time for partial scan process is reduces Maximum testing length is reduced at 284.Here we were test the ISCAS-85 C432 27benchmark interrupt controller by using BIST circuit.

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