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REALIZATION OF XOR AND XNOR GATES USING QCA BASIC GATES

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ABSTRACT

Quantum dot cellular automata is an emerging nanoelectronic computational architecture which has the potential of faster speed, smaller size and minimum power consumption compared to transistor-based technology. In QCA, binary information are encoded as electronic charge configuration of a cell. Fundamental unit in building of QCA circuit is a QCA cell. A QCA cell is an elementary building block which can be used to build basic gates and logic devices in QCA architecture. This paper presents the implementation of XOR and XNOR gates using QCA basic gates i.e. 3 input majority voter gate and inverter. Quantum dot cellular automata is an emerging nanoelectronic computational architecture which has the potential of faster speed, smaller size and minimum power consumption compared to transistor-based technology. In QCA, binary information are encoded as electronic charge configuration of a cell. Fundamental unit in building of QCA circuit is a QCA cell. A QCA cell is an elementary building block which can be used to build basic gates and logic devices in QCA architecture. This paper presents the implementation of XOR and XNOR gates using QCA basic gates i.e. 3 input majority voter gate and inverter.

Keywords QCA , nanoelectronic, XOR,XNOR.

[1.] INTRODUCTION

VLSI technology has progressed remarkably. However these progresses may slowdown in future. Among the chief technological limitations for this slowdown are the interconnect problem and power dissipation. As more and more devices are packed into the same area, the heat generated during a switching cycle can no longer be removed and may result in damage to the chip. Interconnections do not scale in concert with device scaling because of the effect of wire resistance and capacitance, giving rise to wiring bottleneck.

QCA [1, 5] provides an alternative to the silicon technology.QCA based circuits have the advantage of high speed, high integrity and low power consumption. Also QCA circuits have the advantage of high parallel processing.

XOR and XNOR gates being the universal gates have huge application in the world of digital logic. They can be used in design and development of specific communication circuits like parity generator and checker, error detection and correction circuits. Not only that, as all circuits can be realized by these two gates, they have always been of special importance to scientists. So far, whenever these gates have been implemented using QCA [3, 4, 6,14], first, they were implemented using basic digital logic gates like AND,OR and NOT and then these gates were implemented using QCA. In this paper, we propose the implementation of XOR and XNOR gates by exploiting the unique features of QCA gates. It is seen that the number of gates required is less than that required when digital logic gates are used.

2. QCA DESIGN SCHEME

The quantum dot cellular automata use a binary representation of information, by replacing the current switch with a cell having a bistable charge configuration. One configuration of charge represents a binary “1", the other a "0", but no current flows into or out of the cell. The field from the charge configuration of one cell alters the charge configuration of the next cell. Remarkably, this basic device-device interaction is sufficient to support general purpose computing with very low power dissipation.

2.1QCA Cells

The essential feature of a QCA cell [2] is that it possesses an electric quadrupole which has two stable orientations as seen in Fig. 1. These two orientations are used to represent the two binary digits, "1" and "0".A QCA cell is a structure comprise of four quantum-dots arranged in a square pattern.QCA information processing is based on the Coulombic interactions between many identical QCA cells.

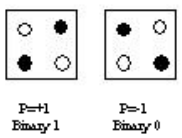

Fig1: Basic QCA cell and Two Possible Polarizations

The cells contain two mobile electrons(or holes) which repel each other as a result of their mutual Coulombic interaction and, in the ground state, tend to occupy the diagonal sites of the cell. These lead to two polarizations

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of a QCA cell, denoted as P=+1 and P=-1 respectively. Thus logic 0 and logic 1 are encoded in polarization P=+1 and P=-1 respectively. When a second cell is placed near the first cell, the coulomb interaction between the cells removes the degeneracy and determines the ground state of the first cell.

2.2QCA Wires

In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells .During each clock cycle, half of the wire is active for signal propagation, while the other half is unpolarized. During the next clock cycle, half of the previous active clock zone is deactivated and the remaining active zone cells trigger the newly activated cells to be polarized. Thus, signals propagate from one clock zone to the next.

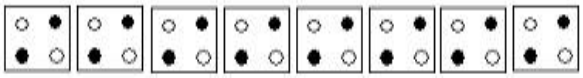


Fig2: QCA Wires

2.3QCA gates

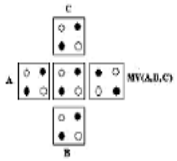
Majority voter gate and inverter acts as the basic gates in QCA. The governing equation of majority voter gate is

$$M(A, B, C) = AB + BC + AC$$

Two input AND and OR gate can be implemented from three input majority voter gate by making one input constant.

$$M(A, B, 1) = A + B$$
$$M(A, B, 0) = AB$$

Fig 3 and Fig 4 shows the gate symbols and their layout.



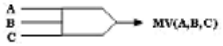
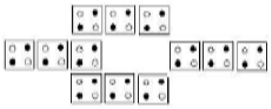


Fig3: QCA Majority Voter Gate



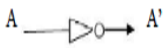


Fig4: QCA Inverter Gate

3. XOR and XNOR Gates

Two-input XOR(exclusive OR) also known as exclusive disjunction is a logical function which gives a high output only if any one of the two inputs but not both are high.

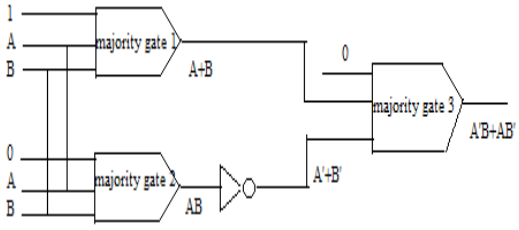
Two-input XNOR is a logical function which gives a high output is both the inputs are high or low.

3.1Proposed Method

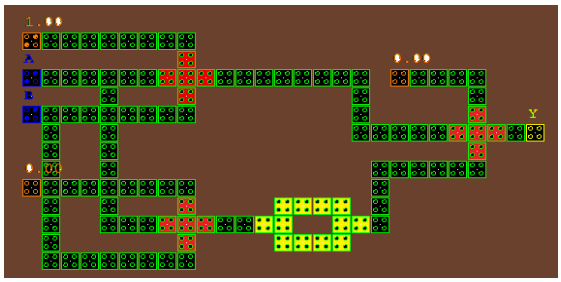
Two-input XOR gate can be realized using three majority voter gate and an inverter. Among these majority gates, two are made to behave like AND gates by making one input line equal to '0' and the third majority gate is made to behave like an OR gate by making the third input line equal to '1'. The governing equation of XOR gate is simplified as follows.

$$Y = (A+B).(AB)'$$
$$= (A+B).(A'+B')$$
$$= A'B + AB'$$

The circuit diagram and the layout of XOR gate is shown in Fig 5(a) and Fig 5(b). The third input line of majority gate 1 is made high and that of majority gate 2 is made low. The output of majority gate 2 is fed into an inverter. Finally, the output from the majority gate 1 and that of the inverter is fed into majority gate 3 whose third input line is made 0. The output of majority gate 3 is the XOR function.



(a): Circuit Diagram



(b): Layout

Fig5: XOR gate using QCA majority gate and inverter (a) circuit diagram (b) layout

Two-input XNOR gate can also be realized using three majority voter gate and an inverter. Among these majority gates, two are made to behave like OR gates by making one input line equal to '1' and the third majority gate is made to behave like an AND gate by making the third input line equal to '0'. The governing equation of XNOR gate is simplified as follows.

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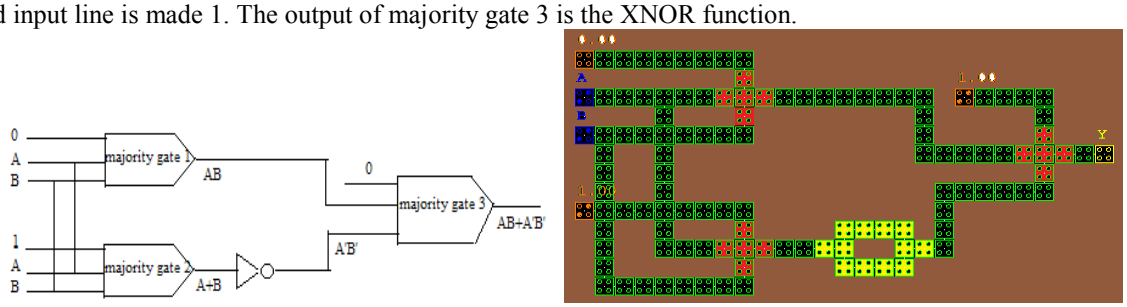
$$Y= (AB)+ (A+B)'$$
$$= (AB)+ (A'B')$$
$$=AB+A'B'$$

The circuit diagram and the layout of XNOR gate is shown in Fig 6(a) and Fig 6(b). The third input line of majority gate 1 is made low and that of majority gate 2 is made high. The output of majority gate 2 is fed into an inverter. Finally, the output from the majority gate 1 and that of the inverter is fed into majority gate 3 whose third input line is made 1. The output of majority gate 3 is the XNOR function.



(a): Circuit Diagram **(b): Layout**

Fig6: XNOR gate using QCA majority gate and inverter (a)circuit diagram (b)layout

Observing carefully, we can see that the basic layout of XOR and XNOR gates are same. Just by changing the polarity of one of the input lines of the majority gates, we can convert XOR gate to XNOR gate and vice versa.

4. RESULTS

Simulation is done using QCADesigner. The simulation result of XOR and XNOR gate is shown in Fig 7 and Fig 8 respectively. Table 1 shows the comparison between the proposed design and the conventional design. Though it is seen from table 1 that the area is slightly greater than that of the conventional design, the cell count and latency is less than that of the conventional method. Moreover, the proposed method succeeds in exploiting the inherent characteristics of QCA basic gates.

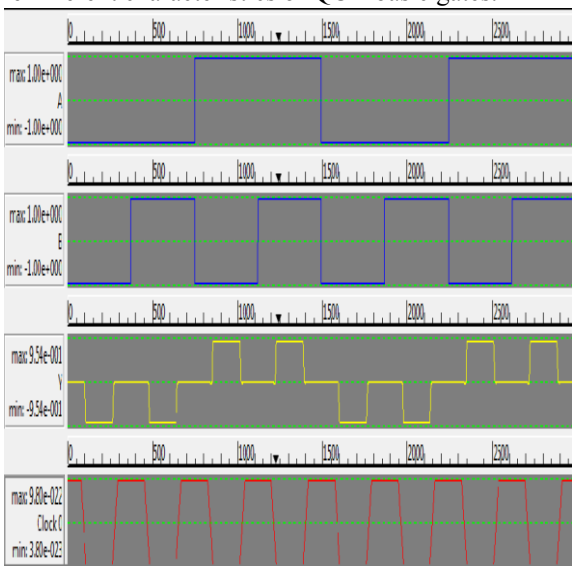


Fig7: Simulation result of XOR gate

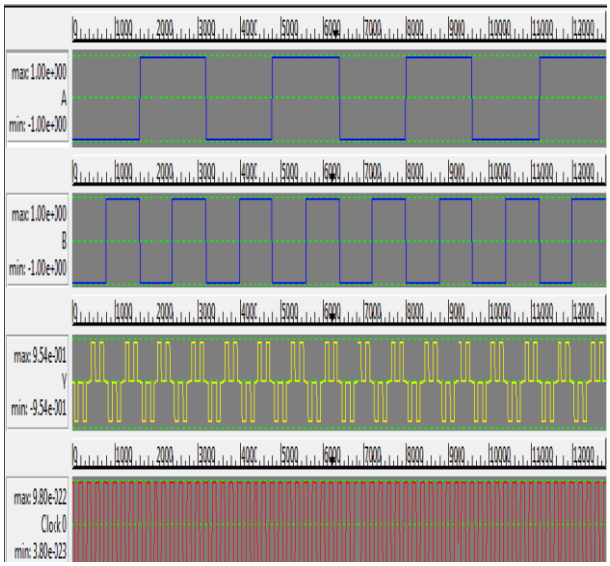


Fig8: Simulation result of XOR gate

Table 1. Comparative study of synthesis of XOR and XNOR gate

Logic structures	Complexity (cell count)	Area (μm^2)	Latency (clock cycles)
Onventional XOR structure	84	0.08	1
Proposed XOR structure	74	0.11	½
Proposed XNOR structure	74	0.11	½

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5. CONCLUSION

This paper proposes the implementation of XOR and XNOR gates by using the inherent characteristics of QCA basic gates. The proposed method shows that without increasing the cell count and area of the circuit, QCA basic gates can be efficiently used to realize the universal gates. Another approach of realizing XNOR gate is by implementing the XOR gate with its output being fed into an inverter. But this would increase the size and complexity of the circuit..

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