A NOVEL DESIGN OF LS-DCCFF FOR LC RESONANT CLOCK DISTRIBUTION NETWORKS

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ABSTRACT

In electronics, the Clock Distribution Networks (CDN) in digital IC’s distributes the clock signal and are operated at high frequencies. So the CDN consumes a large amount of total power in synchronous systems. The need for low-power has caused a major paradigm shift where power dissipation has become as an important consideration as performance and area. Here we introduce a new flip-flop for use in a low-swing LC resonant clocking scheme. The proposed low-swing differential conditional capturing flip-flop (LS-DCCFF) operates with a low-swing sinusoidal clock through the utilization of reduced swing inverters at the clock port. The functionality of the proposed flip-flop was verified at extreme corners through simulations with parasitic extracted from layout. The LS-DCCFF enables 6.5% reduction in power compared to the full-swing flip-flops. The functionality of the proposed flip-flop was tested and verified in TSMC 0.18µm CMOS technology. Low-swing resonant clocking achieved around 5.8% reduction in total power. This CDN circuit using LS-DCCFF can be employed in applications where low power consumption plays a vital role.

Keywords: Delay, flip-flop, Low-swing, power, resonant-clock

[1] INTRODUCTION

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability. Power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. Several factors have contributed to this trend. Perhaps the primary driving factor has been the remarkable success and growth of the class of personal computing devices and wireless communications systems which demand high-speed computation and complex functionality with low power consumption. Latest developments in integrated circuit design specifically in 3-D integration where multi-plane synchronization is required, lead us to believe that the power consumption of the CDN will remain at these high levels [3]. The clock buffers are removed to allow the global and local clock energy to resonate between the inductor and entire clock capacitance including the receiving end flip-flops thus enabling maximum power savings [4]. In addition, removing the clock buffers simplifies LC low-swing clocking since only reduced swing buffers are used at the flip-flop gate and not in intermediate levels within the clock tree [7]. In this work, we introduce a low-swing differential conditional capturing flip-flop (LS-DCCFF) for use in low-swing LC resonant CDNs. As far as, this is the first application of low-swing clocking to LC resonant CDNs. In our approach, no additional power supply is required to achieve low-swing clocking. We have characterized a frequency dependent delay associated with the pulsed flip-flop with a low-swing sinusoidal clock. We also provide measurement results from an integrated test chip fabricated in TSMC 180-nm CMOS technology. Furthermore, we report the power savings achievable through low-swing clocking.

2. CLOCK DISTRIBUTION NETWORKS (CDN)

CDNs in synchronous digital integrated circuits that deliver the clock signal that controls the flow of data within the system. The input at each clock sink, i.e., flip-flop, is captured at the rising or falling clock edge (single-edge triggered flip-flops), or on both edges of the clock (dual-edge triggered flip-flops), or based on the voltage level of the clock (latches). The main objectives in the design of CDNs are to minimize skew, jitter, and power. CDN power dissipation can be expressed as

\[ P = \alpha f CLVddVSW \]  \hspace{1cm} (1.1)

- \( \alpha \) is the switching activity
- \( f \) is clock frequency
- \( CL \) is clock load Capacitance
- \( Vdd \) is the supply voltage
- \( VSW \) is the clock voltage swing.
An attractive approach to reduce power is to scale down the supply voltage which has a quadratic effect on power consumption. Various clock distribution structures have been developed given that the routing area and complexity, speed and power dissipation of the system are all factors affected by the clock network design. Fig. 1 illustrates common CDN structures. An asymmetric buffered tree structure is shown in Fig. 1(a). In this structure, the wire as well as the buffer delay is balance in each path in order to achieve zero skew at the clock leaves. When the clock sinks are uniformly distributed, a symmetrical tree structure is used such as the H- and X-tree structures shown in Figure 3.1(b), (c). Clock grid or mesh Figure 3.1(d) is another alternative to distribute the clock signal. The mesh actively reduces skew by connecting path resistances in parallel.

### 3. DESIGN OF MODIFIED LS-DCCFF

Conditional capturing is used to minimize flip-flop power at low data switching activities by eliminating redundant internal transitions. Fig. 2 LS-DCCFF operates in a pre-charge and evaluate fashion. Pull-up PMOS transistors are used for charging nodes SET and RESET. The effects of charge sharing can be reduced by ensuring a constant path to VDD. This is done by properly sizing the PMOS transistors. A short evaluation interval occurs after the rising edge of the clock when both the clock and inverted clock signals applied to transistors MN1/MN2 are above the threshold voltage level of the NMOS transistor. The DCCFF uses a NAND latch for storage.

Using feedback from the output to control transistors MN3 and MN4 in the evaluation paths ensures conditional capturing. Therefore if the state of the input data is not changed, SET and RESET are not discharged. The load PMOS transistor in the reduced swing inverters is always in saturation since \( V_{gs} = V_{ds} \). The peak voltage for the low-swing clock was chosen to be equal to 0.65V since the threshold voltage of the PMOS transistor is approximately 0.34V. The LS-DCCFF presented in Fig. 3 was modified at node X to allow the operation under full- and low-swing clocking. When signal FULL_SWING is high, full-swing clocking is enabled and the inverted clock output of the normal inverters \( CLKD_{FS} \) is feeding transistor MN1. Whereas low-swing clocking is enabled when signal FULL_SWING is low and the output of the reduced voltage swing inverters \( CLKD_{LS} \) feeds transistor MN1.

### 4. SIMULATION RESULTS

The simulation results for both conventional and proposed LS-DCCFF in this chapter. Simulation of the conventional flip-flop design is done using the Mentor Graphics EDA tool TSMC 0.18\( \mu \)m technology. The
schematic diagram of the design is drawn using the pyxis schematic and the layout is drawn using the pyxis layout. Let $V_1$ (CLK), $V_2$ (I1) and $V_3$ (I2) be the input signals and let $V_4$ (O1) and $V_5$ (O2) be the output signals. When $V_1$ (CLK), $V_2$ (I1) and $V_3$ (I2) are given full-swing (1VDD), $V_4$ (O1) and $V_5$ (O2) are obtained in mV. The total power dissipation for this model is 20631.35pW. The simulation wave of this model is shown in Fig.4.

Simulation of the proposed flip-flop design is done using the Mentor Graphics EDA tool TSMC 0.18µm technology. The schematic diagram of the design is drawn using the pyxis schematic and the layout is drawn using the pyxis layout. Let $V_6$ (CLK), $V_7$ (FS), $V_2$ (I1) and $V_3$ (I2) be the input signals and let $V_4$ (O1) and $V_5$ (O2) be the output signals. When $V_6$ (CLK), $V_7$ (FS), $V_2$ (I1) and $V_3$ (I2) are given low-swing (0.65VDD), $V_4$ (O1) and $V_5$ (O2) are obtained in mV. The total power dissipation for this model is 878.218pW. The simulation wave of this model is shown in Fig.5.

The layout designed for proposed model is shown in the figure 6. The layout is designed using the pyxis layout. From the layout drawn, area occupied by this model is estimated as 478.25 µm².
CONCLUSION

From the simulation results shown for conventional and proposed model, it is very clear that proposed model has given the low power as well as low area. The proposed model is more efficient than the conventional model. The scheme in the proposed model has a power management system based on automatic amplitude control; that can be used to insure the integrity of the generated clock with the desired peak voltage. After analyzing the performance of proposed LS-DCCFF using Mentor Graphics EDA tool under TSMC 0.18µm CMOS technology, it was found to occupy less area of 478µm² and low power of 878.218PW.

REFERENCES