A Low Power 2/3 Prescaler Using Pass Transistor Logic with Integrated P&S Counter
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ABSTRACT
An easier force single-stage clock multiband adaptable divider with joining together P&S counter is displayed. Changed manifestation of augmented accurate single-stage clock (E-TSPC) based gap by-2/3 counter was planned utilizing pass transistor rationale, which requires stand out transistor to execute both the numbering rationale and the mode determination control. This technique has been investigation progressively provision. In Existing strategy differentiate P and S –counters are utilized. Here flip-tumbles and door check are utilized to outline a 2/3 prescaler. In this paper productive multiband adaptable divider for Bluetooth, Zigbee and remote principles dependent upon the beat swallow topology. Contrasted with the existing strategy the changed circuit lessens the intricacy, power utilization & entryway checks and so forth.
Index term: - Dual modulus prescaler, Extended true single-phase clock (E-TSPC), multiband divider, Wireless body network (WBN), Low power, programmable (P) counter, Swallow (S) Counter.

1. INTRODUCTION
Wireless LAN in the multigigahertz bands, such as IEEE 802.11a/b/g are recognized as leading standards for high-data rate transmissions and standards like IEEE 802.15.4 are recognized for low-data rate transmissions. The frequency synthesizer was usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer. The first-stage frequency divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range. The use of short range wireless communications created new protocols that define all parts of communication net-work including physical layer. The emerging of wireless sensor and telemetry network systems, such as ZigBee, demands for low-power low-cost wireless radio-frequency transceivers, in order to achieve long operation time. Technical requirements, e.g. phase noise and channel spacing, for short-range, low data rate wireless communication systems are much relaxed. Therefore power dissipation is the most important requirement. Frequency synthesizer is one of the most critical and power-hungry components in wireless transceiver.

The rapid evolution of the communications industry has greatly increased the demand for lower cost, lower power and wider bandwidth RF circuits operating at microwave frequencies with higher level of integration. In the previous design, a dynamic logic multiband flexible integer-N/N+1 divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multimodules32/33/47/48. In this paper a new method for designing a dynamic logic multiband flexible integer-N/N+1 divider has been proposed which was developed using a wideband multimodules 32/33/47/48 prescaler with a pass transistor based low-power wideband 2/3 prescaler and an integrated P & S counter as show in fig 1. Swallow counter (S-counter) which was used in design has been replaced by a simple digital circuit. This paper has been implemented in real time application in a WBAN radio transceiver. In the transmitter block, the physical layer service data unit (PSDU) from the MAC layer is processed in the proposed transmitter (TX) baseband processor module to generate a physical layer protocol data unit (PPDU) packet. The channel coding and signal processing are performed on the PPDU in the TX baseband processor module, and the raw data rate of the TX baseband processor module output is 250 kb/s. The baseband raw data is modulated by FSK and then directly up-converted to a 2.45 GHz RF signal. In the receiver (RX) block, the received RF signal is down-
converted to a 2 MHz intermediate frequency (IF) signal and then demodulated by a low power FSK demodulator. The demodulated signal is processed by the proposed RX baseband processor module. Following that, the received PSDU is fed into the MAC layer.

2. SURVEY OF EXISTING METHODS

In [1] a dynamic logic multiband flexible integer divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multimodulus 32/33/47/48 prescaler. The divider also uses an improved low-power loadable bit-cell for the Swallow 5-counter. The existing prescaler performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider. It’s consisting of separate programmable (P) counter and swallow (S) counter.

2.1 Dynamic-logic frequency divider

The adoption of dynamic dividers in CMOS phase-locked loops for multigigahertz applications allows to reducing the power consumption substantially without impairing the phase noise and the power supply sensitivity of the phase-locked loop (PLL). A 5-GHz frequency synthesizer integrated in 0.18-m CMOS technology demonstrates a total power consumption of 13.5 mW [6]. The frequency divider combines the conventional and the extended true-single-phase-clock (ETSPC) logics. The oscillator employs a rail-to-rail topology in order to ensure a proper divider function. This PLL intended for WLAN applications can synthesize frequency between 5.14 and 5.70 GHz in step of 20 MHz the reference spurs at 10-MHz offset are as low as 70dBc and the phase noise is lower than 116dBc/Hz at 1MHz over the whole tuning range. The programmable divider in the feedback branch employs the pulse-swallow architecture. The stages inside the dashed box in Fig. 1 are realized in TSPC logic, while the swallow counter is in static CMOS logic. The most critical block of the programmable divider is the +8/9- prescaler, whose structure is shown in Fig. 2. In order to relax the speed constraints of this prescaler, its input frequency is first halved by a fixed-ratio +2 divider. This solution forces to reduce the reference frequency to half of the channel spacing, i.e., 10MHz.

2.2 Dual-band fast-locked frequency synthesizer

This paper presents a fully integrated 1-V, dual band, fast-locked frequency synthesizer for IEEE 802.11 a/b/g Wireless LAN applications. It can synthesize frequencies in the range of 2.4-2.7 GHz with a step of ±9.375 MHz, and in the range of 5.14-5.70 GHz with a step of 20 MHz. Simulation using 0.18-m CMOS technology demonstrates a total power consumption of 7 mW. An adaptive bandwidth controller was employed to achieve a fast locking time. The frequency divider combines the conventional and the extended true-single-phase-clock (ETSP) logics. To ensure a proper dividing function, a cascade voltage switch (CVS) topology is used in the prescaler stage. The reference spurs at an set of 10-MHz are as low as -80 dBc, and the phase noise at an set of 1 MHz is lower than -118 dBc for the entire tuning range.

2.3 Extended true single-phase clock-based prescaler

The power consumption and operating frequency of the Extended True Single-Phase Clock (ETSPC) based frequency divider was investigated. The short-circuit power and the switching power in the ETSPC-based divider are calculated and simulated. A low-power divide-by-2/3 unit of a prescaler is proposed and implemented using a CMOS technology. Compared with the existing design, a 25% reduction of power consumption was achieved. A divide-by-8/9 dual-modulus prescaler implemented with this divide-by-2/3 unit using a 0.18-m CMOS process was capable of operating up to 4 GHz with low-power consumption. The prescaler was implemented in low-power high-resolution frequency dividers for Wireless LAN applications.

2.4 Injection-locked frequency divider

A phase-locked loop (PLL) based frequency synthesizer at 5 GHz is designed and fabricated in 0.18-m CMOS technology. The power consumption of the synthesizer is significantly reduced by using an injection-locked frequency divider (ILFD) as the first frequency divider in the PLL feedback loop. The synthesizer chip consumes 18mW of power, of which only 3.93mW is consumed by the voltage-controlled oscillator (VCO) and the ILFD at 1.8-V supply voltage. The VCO has the phase noise of 104dBc/Hz at 1-MHz offset and an output tuning range of 740MHz. The chip size is 1.1 mm×0.95 mm. Typical architectures of RF frequency synthesizer include integer-frational and dual loop. Among them, the integer-architecture is the most popular one, but its loop bandwidth is limited because the reference frequency must be equal to the channel spacing. Thus, low reference frequency and high division ratio must be used in the feedback loop of an integer-architecture. However, the channel spacing of IEEE 802.11a is 20 MHz, which is wide enough to relax the earlier constraint. Hence the integer-architecture will be adopted in this paper.

3. DIVIDE BY 2/3 COUNTER DESIGN

The two FFs and the AND gate are common in existing designs. The OR gate for the divide control is replaced with a switch show in fig 2. Note that there is a negation bubble at one of the AND gate’s input. The output of
FF1 is complemented before being fed to FF2. When the switch was open, the input from FF1 is disconnected and FF2 alone divides the clock frequency by 2. When the switch is close, FF1 and FF2 are linked to form a counter with three distinct states as shown in Fig.3. According to the simulation results given, E-TSPC design shows the best speed performance in various counter designs including the one using conventional transmission gate FFs.

When the switch is open, the input from FF1 is disconnected and FF2 alone divides the clock frequency by 2. When the switch was close, similar to the existing design, FF1 and FF2 are linked to form counter with three distinct states. E-TSPC FFs are particularly useful for low voltage operations because of the minimum height in transistor stacking. Other than the two E-TSPC FFs, only one PMOS transistor is needed. The PMOS transistor controlled by the divide control signal serves as the switch. The AND gate plus input inverter are achieved by the way of wired-AND logic using no extra transistors at all. The proposed design scheme is far more sophisticated than the measure of simply adding one pass transistor. First of all, unlike any previous designs, the E-TSPC FF design remains intact without any logic embedding. Both speed and power behaviors are not affected, which indicates a performance edge over the logic embedded flip-flop design. Secondly, the inverter to complement the one of the two E-TSPC FF outputs for divide-by-3 operations was removed in the proposed design. The circuit simplification, again, suggests the improvements in both speed and power performances. The working principle of the proposed design is elaborated as follows. When DC is “1”, the PMOS transistor PDC is turned off as a switch should behave. A single PMOS transistor, however, presents a smaller capacitive load to FF1 than an inverter does in design. When DC is “0”, the output of FF1, Q1b, is tied with the output node of the 1st stage inverter of FF2 through the PMOS transistor. In an E-TSPC FF design, the output of the first stage inverter can be regarded complementary to the input D, i.e., D. Therefore, a wired-OR logic is fact implemented. Either Q2b being “0” or Q1b being “1” pulls the output node of the inverter high. This means $D2b = Q1b + Q2b$. By applying Demorgan’s law to the Boolean equation gives rise to $D2b = D2 = \overline{Q1}$. Q2 which is exactly the desired logic. Since Q1b is applied to the input of D, the inverter needed to complement the Q1b signal can be eliminated.

![Fig. 2: E-TSPC-based Logic structures of divide-by-2/3 counter design.](image)

![Fig. 3. MOS schematics of divide-by-2/3 counter design with pass transistor logic circuit technique](image)

## 4. Units Multimodulus 32/33/47/48 Prescaler

The proposed wideband multimodulus prescaler is similar to the 32/33 prescaler, but with an additional inverter and a multiplexer. The proposed prescaler can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 4. It performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider. The multimodulus prescaler consists of the wideband 2/3 (N1 / (N1 + 1)) prescaler, four asynchronous E-TSPC divide-by-2 circuits (AD) = 16) and combinational logic circuits to achieve multiple division ratios. Besides the usual MOD signal for controlling N / (N + 1) divisions, the additional control signal Sel is used to switch the prescaler between 32/33 and 47/48 modes.

### 4.1 Case 1: Sel = 0

When Sel = 0, the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates the normal 32/33 prescaler, where the division ratio was controlled by the logic signal MOD. If MC = 1, the 2/3 prescaler operates in the divide-by-2 mode and when MC = 0, the 2/3 prescaler operates in the divide-by-3 mode. If MOD = 1, the NAND2 gate output switches to logic “1” (MC = 1) and the
wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio $N$ performed by the multimodulus prescaler is

$$N = (AD \times N1) + (0 \times (N1 + 1)) = 32 \quad (1)$$

Where $N1 = 2$ and $AD = 16$ is fixed for the entire design. If $MOD = 0$, for 30 input clock cycles $MC$ remains at logic “1”, where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, $MC$ remains at logic “0” where the wideband prescaler operates in the divide-by-3 mode. The division ratio $N + 1$ performed by the multimodulus prescaler is

$$N + 1 = ((AD - 1) \times N1) + (1 \times (N1 + 1)) = 33 \quad (2)$$

Fig. 4 : Multimodulus 32/33/47/48 Prescaler

4.2 Case 2: $Sel = 1$

When $Sel = 1$, the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal. If $MC = 1$, the 2/3 prescaler operates in divide-by-3 mode and when $MC = 0$, the 2/3 prescaler operates in divide-by-2 mode which was quite opposite to the operation performed when $Sel = 0$. If $MOD = 1$, the division ratio $N + 1$ performed by the multimodulus prescaler is same as except that the wideband prescaler operates in the divide-by-3 mode for the entire operation given by

$$N + 1 = (AD \times (N1 + 1)) + (0 \times N1) = 48 \quad (3)$$

If $MOD = 1$, the division ratio $N$ performed by the multimodulus prescaler is

$$N = ((AD - 1) \times (N1 + 1)) + (1 \times N1) = 47 \quad (4)$$

5. INTEGRATED P AND S COUNTER

Fig. 5 shows as the block diagram of Integrated P&S counter. As it is apparent, this counter consists of a divide-by-128 (P counter) that is made up of 7 divide-by-2. Digital circuit consists of XNOR gates (X0 – X5), AND gates (A1, A2) and a RESETSET Flip Flop (RSFF). This digital section has replaced S counter in conventional ones and has the duty to control modulus bit of dual modulus prescaler. A1 gate is driven by XNOR gates (X0 – X5). When inputs of XNOR are equal (both of them are 0 or 1), output of XNOR gate is logic one. So when the value of P counter (P6P5P4P3P2P1P0) is equal to predefined C number (C1C5C4C3C2C1C0), output of A1 gate becomes logic 1 (CC5-C0 bits are defined by transceiver system that changes the frequency channel of PLL). In this moment, as $P6$ is 1 as well, RSFF was set by A2 gate and dual modulus prescaler divide input frequency by N. When P6 changes to 0, RSFF is reset and dual modulus prescaler return to divide-by-(N + 1) state. For more details, assume the P counter is ZERO condition {P6P5P4P3P2P1P0=0000000}. As $P6$ is equal to 0, RSFF is reset and dual modulus prescaler divides input frequency by (N + 1). In order for the PLL to work in 6th frequency channel and we load the number of 6 on C5-C0 {C5C4C3C2C1C0=000110}. Input signal is applied and $P$ counter increases until the value of P counter reaches the predefined C {P6P5P4P3P2P1P0=1C5C4C3C2C1C0}. (For this example: P6P5P4P3P2P1P0=1000110). In this value of P counter, output of XNOR blocks and $P6$ are logic 1 that causes RSFF to be set by A1 and A2 gates. After this time, the prescaler divide input frequency by N till the P counter reaches to its maximum value (1111111) and next value is 0000000. RSFF is reset by P6, prescaler returns to divide-by- (N + 1) situation and the cycle repeats again. In this cycle the events occurred similar to conventional pulse Swallow divider. For the quantity of predefined C (C1C5C4C3C2C1C0=C), prescaler divide input frequency by (N + 1) and for rest of number (128 – C) its divide the input frequency by N. For a cycle will have.

5.1 Case 1: $Sel = 0$

The frequency division (FD) ratio of the multiband divider in this mode is given by

$$FD = (N + 1) \times S + N \times (P - S) = NP + S$$

Substituting $P = 128$, $S = C$ in the above equation, we get:

$$FD = N \times 128 + C \quad (5)$$

5.2 Case 2: $Sel = 1$

The frequency division (FD) ratio of the multiband divider in this mode is given by

$$FD = (N \times S) + (N + 1) \times (P - S) = (N + 1) P - S$$

Substituting $P = 128$, $S = C$ in the above equation, we get

$$FD = (N \times S) + (N + 1) \times (P - S) = (N + 1) P - S \quad (7)$$
FD = (N + 1)* 128 – C \hspace{1cm} (8)

Fig. 5: Integrated P&S counter (7 bit P-counter and 6 bit programmable S-counter)

6. APPLICATION
A body area network (BAN), also referred to as a wireless body area network (WBAN) or a body sensor network (BSN), is a wireless network of wearable computing devices. In particular, the network consists of several miniaturized body sensor units (BSUs) together with a single body central unit (BCU). A WBAN system can use WPAN wireless technologies as gateways to reach longer ranges. A low power low data rate digital baseband transceiver IC is proposed, which uses low-complexity architecture to achieve satisfactory performance. The target power consumption is less. Benefiting from the novel low complexity hardware architecture design and optimized hardware implementation. Specified physical layer (PHY) architecture is developed, which reduces the complexity of baseband processing but maintains satisfactory performance. To recover precisely the timing and data information from an FSK demodulator, a novel synchronization and data recovery (SDR) scheme is proposed that has comparatively low complexity.

Fig. 6: Wireless body area network based on multiband flexible divider

The complete system diagram of a WBAN radio transceiver is shown in Fig. 6. In the transmitter block, the physical layer service data unit (PSDU) from the MAC layer is processed in the proposed transmitter (TX) baseband processor module to generate a physical layer protocol data unit (PPDU) packet. The channel coding and signal processing are performed on the PPDU in the TX baseband processor module, and the raw data rate of the TX baseband processor module output is 250 kb/s. The baseband raw data is modulated by FSK and then directly up-converted to a 2.45 GHz RF signal. In the receiver (RX) block, the received RF signal is down-converted to a 2 MHz intermediate frequency (IF) signal and then demodulated by a low power FSK demodulator. The demodulated signal is processed by the proposed RX baseband processor module. Following that, the received PSDU is fed into the MAC layer.

7. SIMULATION RESULT
The simulation of the design is performed using Xilinx and Modelsim. The proposed multiband flexible divider consumes power of 109 mw and has a gate count of 2,684. The power consumption, gate count and area of the previous programmable dividers and the proposed programmable divider at the supply voltage of 1.8V is shown in Table I
CONCLUSION
In this paper, an easier force single-stage clock multiband adaptable divider with coordinated P&S counter is outlined. The Swallow counter which expends a substantial allotment of vigor in tried and true recurrence divider is reinstated by a straightforward advanced area in this structure. Additionally, the pass transistor based separation by-2/3 counter effectively disentangles the control rationale and one PMOS transistor alone serves the reasons of both mode select and counter excitation logic. Also, the constant requisition has been actualized in Wireless body area network (WBAN). In the paper, the circuit effortlessness prompts diminished force utilization, decreased number of entryways obliged and henceforth a lessened territory prerequisite.

REFERENCES