ANALYSIS AND DESIGN OF LOW POWER SCAN D FLIP FLOP BASED ON POSITIVE EDGE TRIGGER

1L. JEGAN, 2S. NAGA SATYAVATHI
1Sr Lecturer, Department of ECE, Sathyabama University, Chennai, India.
2Department of ECE, Sathyabama University, Chennai, India.
Jegan25@hotmail.com, nagasatyavathi.sn@gmail.com

ABSTRACT
Power dissipation of IC during test mode is greater than the IC’s normal mode of functioning. Power consumption in scan based testing is high due to the toggling of the combinational logic during the scan shift in digital systems. Power reduction is the most critical issue. A FLIP FLOP is a one bit storage device used for storage purpose. Mostly used d-flip flop in digital circuits has been modified in this paper introducing SCAN D FLIP FLOP. This reduces the power by avoiding unnecessary states. SCAN D Flip flop has high speed compare to normal D Flip flop. The Scan D flip flop is introducing in 130nm technology used on the positive edge trigger clock pulse.

Index Terms— CMOS, MOSFET, Positive Edge Triggered D-flip flop, Power Consumption, Delay.

I. INTRODUCTION
Adding more features into a single chip also increases the complexity which demands highly testable circuitries. Therefore, inserting scan chain throughout the entire chip is a technique which cannot be ignored anymore. During the test mode a known set of test vectors are loaded into the scan chain to test the combinational logic between pipeline stages. If there was no scan chain in the circuit the entire chip would have had to run for multiple cycles to send the test results to the chip boundary. Stitching flops makes it possible to serialize the test results and send them through the scan chain. The timing of a design significantly depends on the speed of these flip-flops and also has a major contribution in the total power consumption of the design. Testing power may be twice as high as the power consumed during normal function mode, because: Successive functional input vectors usually have significant correlations than the correlations between consecutive test patterns. Test engineers usually use parallel testing in the system to reduce the test application time thus cut the test cost, which leads to excessive power dissipation in the long duration of shift phase. Scan-based test techniques dominate the current Design for Testability (DFT) market, but they suffer from increasing power dissipation caused by excessive transitions during test vector shift and capturing processes, which will create unnecessary transitions in the cores under test (CUT). This excessive power dissipation causes the CUT fail or damage during testing period itself. Therefore, the demand of low power testing technique is necessary.

The testing of sequential circuits is complicated because of the difficulties in setting and checking the states of the memory elements. These problems can be overcome by modifying the design of a general sequential circuit so that it will have the following properties:

1. The circuit can easily be set to any desired internal states.
2. It is easy to find a sequence of input pattern such that the resulting output sequence will indicate the internal state of the circuit. In other words: the circuit has a distinguishing sequence.

An important FLIP FLOP function for ASIC testing is called SCAN capability. The idea is to be able to drive the FLIP FLOPs. D input with an alternate source of the data during drive testing. When all the flip flops put into the testing mode, a test pattern can be “scanned in” to the ASIC using the flip flops alternative data inputs. After the test pattern is loaded, the flip-flops are put back into “normal” mode, and all of the flip flops are clocked normally. After one or more clock ticks, the flip-flops are back into test mode and the test result are “scanned out”.

II. POSITIVE EDGE TRIGGERED SCAN D FLIP FLOP

Figure 1.1 (a) D Flip Flop (b) Scan D flip flop

ILPOSITIVE EDGE TRIGGERED SCAN D FLIP FLOP
You can choose from a number of different scan types, or scan architectures. DFT Advisor, the Mentor Graphics internal scan synthesis tool, supports the insertion of mux-DFF (mux-scan), clocked-scan, and LSSD architectures. Additionally, DFT Advisor supports all standard scan types or combinations therefore, in designs containing pre-existing scan circuitry. You can use the type of scan architecture you want inserted in your design.

Each scan style provides different benefits. Mux-DFF or clocked-scan are generally the best choice for designs with edge-triggered flip-flops. Additionally, clocked-scan ensures data hold for non-scan cells during scan loading. LSSD is most effective on latch-based designs.

The following subsections detail the mux-DFF, clocked-scan, and LSSD architectures.

A. Clocked-Scan

The clocked-scan architecture is very similar to the mux-DFF architecture, but uses a dedicated test clock to shift in scan data instead of a multiplexer. Figure 1.3 shows an original design flip-flop replaced with clocked-scan circuitry.

![Fig.1 clocked scan replacement](image1)

In normal operation, the system clock (sys_clk) clocks system data (data) into the circuit and through to the output (Q). In scan mode, the scan clock (sc_clk) clocks scan input data (sc_in) into the circuit and through to the output (sc_out).

B. LSSD

LSSD, or Level-Sensitive Scan Design, uses three independent clocks to capture data into the two polarity hold latches contained within the cell. Figure 1.4 shows the replacement of an original design latch with LSSD circuitry.

![Fig.2 LSSD Replacement](image2)

In normal mode, the master latch captures system data (data) using the system clock (sys_clk) and sends it to the normal system output (Q). In test mode, the two clocks (Aclk and Bclk) trigger the shifting of test data through both master and slave latches to the scan output (sc_out).

There are several varieties of the LSSD architecture, including single latch, double latch, and clocked LSSD.

C. MUX-DFF:

A mux-DFF cell contains a single D flip-flop with a multiplexed input line that allows selection of either normal system data or scan data. Figure 1.2 shows the replacement of an original design flip-flop with mux-DFF circuitry.
In normal operation (sc_en = 0), system data passes through the multiplexer to the D input of the flip-flop, and then to the output Q. In scan mode (sc_en = 1), scan input data (sc_in) passes to the flip-flop, and then to the scan output (sc_out).

**Why I chose SCAN MUX-DFF:**

In scan architectures the scan MUX-DFF is easy to test the circuit compared to the other two architectures. Why because the scan MUX-DFF contains only one clock, but Clocked-scan contains two clocks. The LSSD is level sensitive, if any change in the transition the circuit output will change. The circuit complexity also less compare to the Clocked-scan and LSSD. So Scan MUX-DFF is better than the other architectures.

**III. POWER DISSIPATION DURING TEST APPLICATION:**

The ever increasing demand for portable computing devices requires low power VLSI circuits. Minimizing power dissipation during the VLSI design flow increases lifetime and reliability of the circuit. Numerous techniques for low power VLSI circuit design were reported for CMOS technology where the dominant factor of power dissipation is dynamic power dissipation caused by switching activity. While these techniques have successfully reduced the circuit power dissipation during functional operation, testing of such low power circuits has recently become an area of concern. Therefore, addressing the problems associated with testing low power VLSI circuits has become an important issue.
IV. POWER REDUCTION METHODOLOGY:

Power dissipation in CMOS circuits consists of two types: dynamic power and static power. Dynamic power dissipation occurs during output switching because of short-circuit current, and charging and discharging of load capacitance, while static power dissipation is caused by leakage current or other current continuously drawn from the power supply. For CMOS technology, dynamic power is the dominant source of power dissipation.

Switching power: Due to charging and discharging of output capacitance.

\[
\text{Energy/transition} = C_L * V_{dd}^2 \\
\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f
\]

Where \( C_L \) = load capacitance (pf) \\
\( V_{dd} \) = supply voltage \\
\( f \) = frequency

Dynamic power dissipation:
CMOS circuits dissipate power by charging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitances) whenever they are switched. In one complete cycle of CMOS logic, current flows from \( V_{dd} \) to the load capacitance to charge it and then flows from the charged load capacitance to ground during discharge. Therefore in one complete charge/discharge cycle, a total of \( Q = C_L V_{dd} \) is thus transferred from \( V_{dd} \) to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage again to get the characteristic switching power dissipated by a CMOS device.

Dynamic power dissipation of CMOS circuit can be calculated as:

\[
\text{Power} = \text{Energy/transition} * \text{transition time} = C_L * V_{dd}^2 * f_{\text{clk}} * \text{switching activity}(
\]

Since most gates do not operate/switch at every clock cycle, they are often accompanied by a factor \( Q_c \), called the activity factor. Now, the dynamic power dissipation may be re-written as:

\[
\text{Power} = C_L * (V_{dd}^2 / 2) * f_{\text{clk}} * \text{switching activity}(Q_c)
\]

Where \( C_L \) = load capacitance (pf) \\
\( V_{dd} \) = supply voltage \\
\( f \) = frequency \\
\( Q \) = switching activity

V. SIMULATION RESULTS

To evaluate the performance, conventional and proposed flip-flop structures discussed in this paper are designed using 130-nm CMOS technology. All simulations are carried out using ELDO simulation tool at positive edge trigger SCAN DFF. The simulated waveform of the proposed SET flip-flop is shown in Fig. 5.

![Fig 5: Transient Analysis edges trigger SCAN D Flip Flo](image)

VI. PERFORMANCE ANALYSIS

The performance of the proposed Positive edge trigger SCAN D-FF is evaluated by comparing the average power, delay and timing constraints for normal flip flop and proposed scan D-FF. The following tables from TABLE 1 to TABLE 3 furnished the performance parameters for power dissipation and propagation delay.
CONCLUSION
The POSITIVE EDGE TRIGGERED D FLIP FLOP is presented in this paper for low power VLSI testing. This proposed scan FF not only saving the power and can also operate with higher speed. The area overhead due to increasing the width of the cell is more, so area is more. This positive edge trigger SDFF can be included into the standard cell library so that any timing violation caused by this FF can be solved in the RTL synthesis level itself

REFERENCES
[1] Dr. Sunil P Khatri and Sivakumar Ganesan,” A Modified Scan-D Flip-flop Design to Reduce Test Power”.  
[6] “A Robust Pulsed Flip-flop and its use in Enhanced Scan Design” Rajesh Kumar_ Kalyana C. Bollapalli_ Rajesh Garg‡ Tarun Soni_ Sunil P. Khatri_ Department of ECE, Texas A&M University, College Station TX 77843.Intel Corporation, Hillsboro, OR 97124