Design and Analysis of Low Power Full Adder Design Using Hd-Logic

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ABSTRACT

The major concern of a VLSI designer is always power, delay and area. The electronics industry has grown to a stage where these three becomes the major constrains for the further development. Due to the integration of millions of components nowadays leakage power and delay tends to play a major role in the total power consumption. Full adder is the major block used as the interblock in many digital signal processors. The major objective of this paper is to overcome the drawbacks of two mode MTCMOS systems. So using the concept of new trimodal logic, full adder is redesigned and analysis is carried out in different nanometer technologies. The difficulty in analysis and power consumption during the usage of this technique can be reduced by the proposed hd-logic. Average power, Delay and Power Delay Product (PDP) of the analysis claims that proposed design is suitable for the low power applications. The hd-logic is a worthwhile work for continuous range of virtual supplies without any data loss and can be used for long standby periods.

Keywords: CMOS, MOSFET, MTCMOS, Full adder, ALU, Trimodal, Data retentive, Power Consumption Virtual ground, Virtual Vdd.

1. INTRODUCTION

The scaling of process technologies to nanometre regime has resulted in a rapid increase in leakage power dissipation. Hence it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactive state. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques for reducing leakage power in sleep or standby mode. But this all techniques shows its own limitations. The use of MTCMOS is in order to optimise the delay or power. MTCMOS consist of multiple voltages such as low threshold voltage devices and high threshold voltage devices. This low threshold devices is used to switch faster the circuits therefore they are very useful in critical path delay to minimise clock periods. But they have higher static leakage power. The high threshold devices reduce static leakage power without incurring the delay penalty. Typical high threshold devices reduce static leakage 10 times compared to low threshold devices. There were mainly two basic approaches in design of MTCMOS, the coarse grained approach and fine grained approach [13]. In coarse grained approach high threshold devices provide voltage to logic blocks then during active mode the transistor will be turned ON and provide virtual power to the low threshold devices. The drawbacks are logic blocks should be partitioned to determine when a block may be safely turned off, sleep transistors must be carefully sized and an always active power management circuit must be added. In fine grained approach high threshold devices are incorporated within every gate but the main drawback here is the area. Power density increases due to the combination of higher clock speeds, smaller feature size and greater functional integration. Thus it becomes a greater challenge for the circuit designers. Even though the designers have a few methods for reducing this static power consumption, these methods have some drawbacks where one has to sacrifice design area and circuit performance. In this paper, we propose a new method to reduce static power in the CMOS VLSI circuit using a Tri-Modal Multi-Threshold CMOS Switch without being penalized in circuit performance. [15]

2. BASICS OF TRIMODAL LOGIC (EXISTING SYSTEM)

MTCMOS technology provides a simple and effective power gating structure by utilizing high speed, low Vt (LVT) transistors for logic cells and low leakage, high Vt (HVT) devices as sleep transistors [13]. Some drawbacks of MTCMOS are long wake up latency, large amount of rush-thru current, and wasteful energy usage during mode transition [15]. In addition, due to data loss in the sleep mode, MTCMOS circuits usually use a data retention strategy to restore the pre-sleep state, which they cannot afford to lose. In particular, regular flip-flops are replaced by retention flip-flops, preserving the pre-sleep state. Retention flip-flops that are larger cells introduce a significant amount of area overhead in designs that require substantial amount of data retention. The circuit configuration of trimodal logic can be explained by two different footer cells such as header and footer cells.
The footer cell provides VVSS to the circuit block. So now the circuit will not be directly connected to the ground. This VVSS is a small voltage which is greater than the ground potential. So here the circuit works under Vdd and VVSS.

The header cell provides VVDD to the circuit block. So now the circuit will not be directly connected to the Vdd. This VVDD is a small voltage given to circuit block placed inside instead of Vdd. Taking the example from daily life, if we need a help from a person who is sleeping (deep sleep mode) he takes more power and time to wake up and to get ready to a normal state to help me, this delay is called wake up latency. But if he was in an intermediate mode then it was easy to make him ready, and this delay can be named as ready latency [13]. So ready latency is less when we compare to wakeup latency. So when it needs to take a transition from sleep to active it takes more power than the state transition from drowsy to active. When a circuit needs to move from sleep mode to active mode, the wakeup latency and the power consumption will be more. During the transition from sleep to active the power consumption will be more if we introduce an intermediate mode the power used will be reduced.[15]

2.1 Regions of Trimodal Logic
The circuit configuration of trimodal logic can be explained by two different cells such as header and footer cells. In this trimodal logic we mainly use the concept of virtual ground (VVSS) and virtual Vdd (VVDD) as shown in fig.1 and fig.2 [15] Instead of providing a Vdd we use to give a virtual Vdd so that the power consumption during the transition period will be less. Likewise instead of providing a proper ground we provide a virtual ground to the circuit so that the leakage power consumption during sleep mode will be less. In active mode all the transistors will be ON and operation will be normal, then the power consumption will be there. Whereas in sleep mode the transistors will be OFF and operation is completely ceased, but still the power consumption will be there which is less compared to the active mode [15].

There are three regions of trimodal operation, of which one region is reasonably a low leakage solution.

<table>
<thead>
<tr>
<th>S0</th>
<th>S1</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>ACTIVE</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>SLEEP</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>DROWSY</td>
</tr>
</tbody>
</table>

The operation can be explained as below:

- **Active Mode**: When sleep = 0, MS1 is ON and there will be a voltage of Vdd at GS node and the circuit attached will start working in a normal condition in between Vdd and Vss.
- **Drowsy Mode**: When sleep=1 and drowsy=1 then it is in drowsy mode. Here MS2 is ON and MD1 is ON and MS is OFF. The transistors both MS and MD2 are OFF and thereby cutting this ground supply voltage.
**Sleep Mode**: When sleep = 1 and drowsy = 1 the circuit block moves to sleep mode. MS2 will be ON and MD1 will be OFF and since MS and MD1 is OFF.

### 2.1.1 Basics of hd-logic

The trimodal logic is far better than a two mode system which works on only active and sleep mode. But the difficulty in redesigning and analysis during the usage of this logic can be reduced when by the use of this proposed hd-logic. Usage of this hd-logic also reduces the power consumption during the state transitions. In footer cell and header cell it makes the circuit block placed inside to work under virtual supplies and normal Vdd or ground. If the circuit block is placed inside a footer cell then it makes the circuit to work under VVSS and Vdd. In this the output waveform will be proper, the power is reduced in the drowsy mode and also during the state transition from drowsy to active mode. If the circuit was under header cell then the circuit placed inside will be working for VVDD and Vss where the power consumption will be much less compared to the footer cell. Since both the footer and header cell is having some drawbacks both the footer and header cell are combined and this combination gave a new drowsy mode (hybrid drowsy mode). Hence this logic is named as hybrid drowsy logic (hd-logic).

![Fig.3. Implementation of hd-logic](image)

Instead of using a drowsy mode, we keep it in a hybrid drowsy mode where the ready latency and power consumption is less. Hence it takes less power during the state transition from hybrid drowsy to active mode. The working principle of hd-logic can be explained using the given Table 2. It describes Sf as sleep signal to the footer cell Sh as sleep signal to the header cell and D as the drowsy signal to the whole circuit. The control signals provided for the circuit will increase efficiency of the performance analysis. All the operations can be done using one circuit itself. The introduction of hybrid drowsy claims that the circuit placed will be suitable for low power applications. Since the power consumption is less during the state transition period, instead of putting a circuit on drowsy mode, we a hybrid drowsy mode.

### Table 2. Switch Operation of hd-Logic

<table>
<thead>
<tr>
<th>Sf</th>
<th>Sh</th>
<th>D</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Half sleep</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Header drowsy</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>Active</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Full sleep</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Hybrid drowsy</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Half sleep</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Footer drowsy</td>
</tr>
</tbody>
</table>
3. REGIONS OF hd-LOGIC
The operation can be explained as below:
- **Half Sleep Mode**: When $S_F=0$, $S_H=0$, $D=0$, MS1 & MS3 will be ON and MD1 & MD3 will ON. Here footer section is in sleep mode.
- **Header Drowsy Mode**: When $S_F=0$, $S_H=0$, $D=1$ then it is in header drowsy mode. Here MS3 & MS1 are ON and MD2 & MD4 are ON. The transistor MV1 is OFF and thereby cutting this power supply voltage. So the circuit will provide virtual Vdd (VVDD) and proper Vss.
- **Active Mode**: When $S_F=0$, $S_H=1$, $D=X$ then MV1 and MV2 are ON and there will be a voltage of Vdd and Vss at the nodes VVDD and VVSS then the circuit attached will start working in a normal condition in between Vdd and Vss.
- **Hybrid Drowsy Mode**: When $S_F=1$, $S_H=0$, $D=1$ the circuit block moves to hybrid drowsy mode. MS2 will be ON and MD1 will be ON and since MS and MD1 is OFF.
- **Half Sleep Mode**: When $S_F=1$, $S_H=1$, $D=0$ the circuit block moves to half sleep mode. MS4 & MS1 will be ON and MV1 & MV2 will be OFF. Here the virtual supplies are given to the circuit to work i.e., instead of Vdd, VVDD is used and instead of Vss, VVSS is used
- **Footer Drowsy Mode**: When $S_F=1$, $S_H=1$, $D=1$ then it is in footer drowsy mode. Here MS4 is ON and MD1 is ON and MV1 is ON. The transistors both MV2 is OFF and thereby cutting this ground supply voltage a virtual supply is provided VVSS.

4. FULL ADDER CELL
Full adder circuit is a functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs. Almost every complex computational circuit requires full adder circuitry. The entire computational block power consumption can be reduced by implementing low power techniques on full adder circuitry. Several full adder circuits have been proposed targeting on design accents such as power, delay and area. This is a full adder using trimodal logic where power can be saved and these full adders are used in ALU.

![Fig.4. Circuit Diagram of Full Adder](image)

The conventional full adder is shown above which is redesigned using the trimodal logic and hd-logic which is completely controlled by the signals sleep and drowsy modes.

5. SIMULATION RESULTS
The entire simulations have been done on 130nm CMOS technology. The simulation result of full adder circuit using trimodal logic is given below.

![Fig.5. Full Adder Using a Trimodal Logic (Sleep To Active)](image)

This Fig.5 depicts a full adder in transition from sleep to active. Here the wakeup latency and ready latency will be more when compared to the transition from drowsy to active. When a circuit need to move from sleep mode to active mode, the wakeup latency and the power consumption will be more. During the transition from sleep to
active the power consumption will be more when compared with the drowsy to active. So if we introduce an intermediate mode the power used will be reduced.

![Fig.6. Full Adder Using A Trimodal Logic (Drowsy To Active)](image)

Fig.6 shows the transition from drowsy to active mode. Here the first condition is 11 so the output is not proper but it is retenting some value. Second condition is active state 01, output will be proper there.

<table>
<thead>
<tr>
<th>TRANSITION</th>
<th>AVG POWER (W)</th>
<th>DELAY(S)</th>
<th>PDP(J)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DROWSY TO ACTIVE</td>
<td>1.809x10^-5</td>
<td>8.28x10^-9</td>
<td>1.49x10^-14</td>
</tr>
<tr>
<td>SLEEP TO ACTIVE</td>
<td>7.518x10^-5</td>
<td>6.32x10^-9</td>
<td>4.75x10^-14</td>
</tr>
</tbody>
</table>

Table 4 shows the PDP during state transition period. Here the power delay product in drowsy to active mode is less when compared to sleep to active.

<table>
<thead>
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CONCLUSION

Full adder circuit is a functional building block and most critical component of complex arithmetic circuits like microprocessors, digital signal processors or any ALUs. This full adder circuit can be redesigned using trimodal logic. This redesigned full adder can be used for redesigning ALU and can be used in digital signal processors. This trimodal logic introduces superior low power solutions across various circuit operating modes using a single circuitry. This mode enables a continuous range of virtual ground voltages. It works for a long standby periods of operation and the data loss in sleep mode can be prevented by keeping the circuit in drowsy mode. According to the simulation results these circuits consume less power, 68.3% of power has been reduced because of the usage of drowsy mode.

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REFERENCES

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