A New High Performance Logic Style for Arithmetic Circuits

K. LINET\(^1\), P. UMARANI\(^1\), T. RAVI\(^1\)
Department of Electronics and Communication Engineering, Sathyabama University, Chennai, India
linetk2910@gmail.com, dhanam.rani09@gmail.com, ravi_vls123@yahoo.co.in

ABSTRACT

A new approach for constant delay logic style is developed in this paper to provide improved power and delay named Low Power High Speed logic (LP-HS logic). Constant delay logic style is examined against the LP-HS logic, by analysis through simulation. It is shown that the proposed LP-HS logic has low power, delay and power delay product over the existing constant delay logic style. A 4 bit ripple carry adder is designed and its performance is evaluated using both existing as well as the proposed logic. The simulation results show that the 4 bit ripple carry adder using LP-HS logic is better in terms of power, delay and power delay product when compared to constant delay logic style. The simulations were done using HSPICE tool in 32nm CMOS technology and performance parameters of power, delay and power delay product were compared.

Keywords: CMOS, MOSFET, VLSI, Power Consumption, Delay, Power delay product (PDP), Constant Delay Logic (CD logic)

1. INTRODUCTION

High performance energy efficient logic style is always important in VLSI circuits. CMOS is the most dominant technology which is used to construct these types of integrated circuits. The most widely accepted parameters to measure the quality of a circuit or to compare various circuit styles are power, delay and area. Advances in CMOS technology have led to improvement in the performance in terms of power, delay and area. There always exists a trade-off between power, delay and area in a circuit. The power delay product is a figure of merit for comparing logic circuit technologies or families. [3] The two different families in the logic style are the static logic and dynamic logic. [13][15]

Static CMOS is the most widely used logic style which consists of pull down network (PDN) and pull up network (PUN). It is truly an extension of the static CMOS inverter with multiple inputs. This logic is static because 1 and 0 are restored by pull up and pull down network respectively. This type of design is having high functional reliability and is very easy to design. Requirement of large implementation area is the major disadvantage of this technique. [12]

Despite its advantages static CMOS suffers from increased area, and correspondingly increased capacitance and delay. Thus we go for pseudo nMOS logic. It is a ratioed logic. [22] The major advantage of this technique is the low area cost which in turn low input gate load capacitance. These forms are not meant to replace complementary CMOS but rather to be used in special applications for some particular purposes. The major drawback of this technique is the non-zero static power dissipation.

Even though pseudo nMOS logic is having many advantages, because of its static power dissipation we go for dynamic logic. Dynamic logic uses a special technique called dynamic precharging. [11] Normally during the time the output is being precharged, the nMOS network should not be conducting. This is usually not possible. Because of the disadvantage of the above logic a new type of dynamic logic called the precharge-evaluation logic is proposed. The drawback of this logic is the charge leakage, charge sharing and cascading problem. Monotonicity problem also exists in case of dynamic logic. [22] In order to mitigate the problems of the dynamic logic several modifications for the existing dynamic logic is made which leads to the introduction of CMOS domino logic, self timed domino logic, NORA domino (NP CMOS) etc.

In order to eliminate the problems associated with the domino logic a new type of logic called feedthrough logic has been introduced. [3][5][6] Basic feedthrough logic is modified in many ways to get rid of the drawbacks associated with them. A new type of feedthrough logic called dynamic feedthrough logic has also been introduced. [19][20] To mitigate the problems associated with the feedthrough logic (FTL) a new high performance logic known as constant delay logic style has been designed. This high performance energy efficient logic style has been used to implement complicated logic expressions. In this paper some modifications have been done for the constant delay logic style to reduce the power consumption and to improve the speed. The proposed technique is known as the LP-HS logic.

2. CONSTANT DELAY LOGIC STYLE

Designers of digital circuits often desire fastest performance. This means that the circuit needs high clock frequency. Due to the continuous demand of increase operating frequency, energy efficient logic style is always important in VLSI. One of the efficient logics which come under CMOS dynamic domino logic is the feedthrough logic (FTL). Dynamic logic circuits are important as it provides better speed and has lesser
transistor requirement when compared to static CMOS logic circuits. Feedthrough logic has low dynamic power consumption and lesser delay when compared to other dynamic logic styles. To mitigate the problems associated with the feedthrough logic new high performance logic known as constant delay (CD) logic style has been designed. [9] It outperforms other logic styles with better energy efficiency. This high performance energy efficient logic style has been used to implement complicated logic expressions. It exhibits a unique characteristic where the output is pre-evaluated before the input from the preceding stage is ready. Constant delay logic style which is used for high speed applications is shown in Fig. 1.

![Constant Delay Logic Style](image)

CD logic consists of two extra blocks when compared to feedthrough logic. They are the timing block (TB) as well as the logic block (LB). Timing block consists of self reset technique and window adjustment technique. This enables robust logic operation with lower power consumption and higher speed. Logic block reduces the unwanted glitch and also makes cascading CD logic feasible. The unique characteristic of this logic is that the output is pre-evaluated before the inputs from the preceding stage got ready. An Nmos pull down network is placed where the inputs are given. Based on the logic which is given in the pull down network we will get the corresponding output.

### 2.1 Buffer Using CD Logic

A buffer circuit implemented using CD logic is shown below. The expanded diagram for timing block as well as logic block is also shown in the Fig. 2.

![Buffer Using CD Logic](image)

The chain of inverters is acting as the local window technique and the NOR gate as a self reset circuit. Length of the inverter chain varies according to the circuit which we have to design. The prime aim of the inverter chain is to provide a delayed clock. The contention problem which is one of the disadvantages of the feedthrough logic is reduced with the help of this window adjustment. In the self reset circuit one of the input of the NOR gate is the intermediate output node X and the other one is the clock. The logic block is simply a static inverter as in the case of dynamic domino logic. Since the above circuit is for a buffer the NMOS pull down network consists of only one nMOS transistor.

### 2.2 Timing Diagram of CD Logic

The timing diagram for constant delay logic is shown in Fig. 3. CD logic works under two modes of operation.

1. Predischarge mode (CLK=1)
2. Evaluation mode (CLK=0)
Predischarge mode happens when CLK is high and evaluation mode occurs when CLK is low. During predischarge mode X and Out are predischarged and precharged to GND and VDD respectively. During evaluation mode three different conditions namely contention, C-Q delay and D-Q delay takes place in the CD logic. Contention mode happens when IN=1 for the entire evaluation period. During this time a direct path current flows from pMOS to PDN. X rises to nonzero voltage level and Out experiences a temporary glitch. C-Q delay (clock-out) occurs when IN goes to 0 before CLK transits to low. At this time X rises to logic 1 and Out is discharged to VDD and the delay is measured from CLK to Out. D-Q delay happens when IN goes to 0 after CLK transits to low. During this time X initially enters contention mode and later rises to logic 1 and the delay is measured from IN to Out.

3. PROPOSED LP - HS LOGIC

The proposed LP-HS logic is derived from the existing constant delay logic. When compared to CD logic there are three major differences in the LP-HS logic. The window adjustment technique is eliminated in this logic. The evaluation transistor is altered as pMOS transistor instead of nMOS. The third variation is the addition of the transistors M2 and M3 in parallel below the pull down network. The proposed logic helps to reduce the power and delay which in turn reduces the power delay product. The circuit diagram for the proposed logic is shown in Fig.4.

Transistors M0 and M1 whose gates are driven by the CLK and the output of NOR gate are connected in series. This increases the resistance which in turn helps reducing the power. M4 is acting as an evaluation transistor. The NOR gate which is behaving as the self resetting logic is constituted by the transistors M5, M6, M7 and M8. M5, M6 and M7, M8 is driven by CLK and the output intermediate node X. IN values are given to the nMOS pull down network which is given according to the circuit which we have to design. Transistors M2 and M3 are connected in parallel and are placed down to the nMOS pull down network. These transistors help to reduce the power delay product. The gate of M2 is driven by the clock and M3 is at ground. Transistor M2 increases the dynamic resistance of the pull down network which successively helps to reduce the power consumption. Transistors M9 and M10 together figures the static inverter which is used to make the cascading logic more feasible.

The circuit works under two modes of operation.

i. Precharge mode (CLK=0)
ii. Evaluation mode (CLK=1)

Precharge mode occurs when clock is low and evaluation mode happens when clock is high. When clock is low, transistor M4 gets ON and provides a high value at node X which in turn provides a low value at the output.
node OUT. When clock is high the transistor M2 gets ON and the nMOS pull down network is evaluated and gives the output. During this time the transistor M0 whose gate is driven by the CLK is in OFF condition. Due to this the contention mode gets wiped out in the evaluation condition which in turn tends for the elimination of window adjustment technique in the proposed logic. One of the reasons for the power and delay reduction in the circuit is the elimination of the window adjustment technique. During the evaluation mode the pull down network and the transistor M2 gets ON which provides high dynamic resistance which further reduces the power. Transistor M3 is in always ON condition which offers an easy discharge of the value to the ground.

4.4 BIT RIPPLE CARRY ADDER

Addition is the fundamental operation for any digital system, digital signal processing or control system. [2][4] A fast and accurate operation of a digital system is greatly influenced by the performance of adders. Adders are also very important component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Full adder is the basic unit of addition employed in all the adder circuits. A full adder (FA) is a combinational circuit that performs the arithmetic sum of three bits: A, B and a carry Cin, from the previous addition. The two outputs are sum S and carry Cout. The ripple carry adder is constructed by cascading full adder blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. [10][16] A 4 bit ripple carry adder (RCA) consists of 4 full adders with the carry signal propagating from one full adder stage from LSB to MSB. The critical path of the ripple carry adder consists of the carry chain from the first full adder stage to the last. A 4 bit ripple carry adder structure is shown in Fig. 5. where x0-x3, y0-y3 represents the two set of inputs. C0 represents carry input. The output sum and carry is shown as S0-S3 and C4 respectively.

5. SIMULATION RESULTS

The design of 4 bit ripple carry adder was simulated using the simulation tool “HSPICE” in 32nm CMOS technology. The operating voltage for 32nm is 0.9V and the operating frequency is kept as 1GHz. The simulation outputs of the 4 bit ripple carry adder using existing as well as the proposed logic is shown below.

Fig.6. Simulation output of Existing 4 Bit Ripple Carry Adder

Fig.6. describes the output waveform of existing 4 bit ripple carry adder in which V(2,3,4,5), V(6,7,8,9) are the two input signals, V(10) refers the carry input. The output sum and carry are represented by V(11,13,15,17) and V(18) respectively.

Fig.7. describes the output waveform of proposed 4 bit ripple carry adder in which V(19) is the clock signal, V(2,3,4,5), V(6,7,8,9) are the two input signals, v(10) refers the carry input. The output sum and carry are represented by V(11,13,15,17) and V(18) respectively.
Table 1. Performance Analysis of 4 Bit Ripple Carry Adder

<table>
<thead>
<tr>
<th>DESIGN</th>
<th>CD LOGIC</th>
<th>LP – HS LOGIC</th>
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<tbody>
<tr>
<td></td>
<td>Power (µw)</td>
<td>Delay (ps)</td>
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<tr>
<td>4 bit RCA</td>
<td>30.03</td>
<td>15.03</td>
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</table>

Table 1 describes the average power consumption, delay and power delay product comparison of 4 bit Ripple Carry Adder in 32nm CMOS technology using both existing system as well as the proposed system.

CONCLUSIONS

The concept of constant delay logic (CD logic) and a modified version of CD logic termed Low Power High Speed logic (LP-HS) is employed to design arithmetic circuits. A 4 bit Ripple Carry Adder is designed using existing and proposed logic. The simulation was carried out in 32nm CMOS technology with an operating voltage of 0.9 V. It is simulated and the performance parameters power, delay, power delay product were compared. The operating frequency was kept at 1GHz. From the results it is found that the power delay product has been improved by 95.56% for 4 bit Ripple Carry Adder using proposed logic.

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