AN EFFICIENT ERROR CORRECTION CODE THAT DEALS WITH ISOLATED DEFECTS

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ABSTRACT

One of the most widely used method of error detection and correction is Single Error Correction and Double Error Detection (SEC-DED) code. With any technology, there is a danger that information will be corrupted due to physical imperfections in storage media or electronic noise. So it is necessary to detect and correct such an erroneous data during transmission. Error detection and correction mechanisms using hamming code play an important role for memory protection. So in this paper an efficient Single Error Correction and Double Error Detection (SEC-DED) methods that deals with isolated defects are introduced.

Keywords: Single error correction, Double error detection, Hamming code

[1] INTRODUCTION

Different types of error correction and detection mechanisms are available. All error detection and correction schemes depending on using more bits to store information than what one actually needs. These extra bits are called parity bits. By using hamming code single error correction and double error detection is possible. But if there is more than two errors, error detection and correction using hamming code is not possible. For Single Error Correction and Double Error Detection (SEC-DED) the minimum hamming distance should be four. There are mainly two types of errors that can be affected by memory data

- Soft errors
- Stuck at defects

Soft errors are the errors; this can be happened during transmission. That is, during transmission because of noise and other interferences the received data will be different from transmitted data. This is mainly because of bit transitions. For example bit 0 will change to bit 1 and bit 1 will change to bit 0. These kinds of errors are called soft errors. Stuck at defects are the faults where the memory cell holds the same value regardless what is supposed to be saved. There are two types of stuck at defects.

- Stuck at -1 defect
- Stuck at -0 defects

Stuck at -1 defect is the defect where the memory cell store always one and where stuck at -0 defect cause the memory cell to store always zero.

Previously there is no any method to correct errors, that is we can just detect if there is any error has occurred or not. For that odd parity and even parity methods for error detection used. Now a day it is possible to detect and correct such an errors by using hamming code. In this paper an efficient Single Error Correction and Double Error Detection (SEC-DED) methods that deals with isolated defects are introduced.

This paper proposes an efficient error correcting technique which deals with isolated defects. For this purpose one of the common error correcting code used, is the SEC-DED code.

This paper explains the already existing error correcting techniques in part II as a review. Then in part III it explains the proposed work and its work flow. In part IV the experimental results and analysis of the work will be discussed. Final part V will be the concluding section of the paper.

2. REVIEW ON ERROR CORRECTING CODES

Hamming R.W in 1950 proposed [8] a family of linear error-correcting codes that generalize the Hamming (7, 4) code. Hamming codes are perfect codes, that is, they achieve the highest possible rate for codes with their block length and minimum distance 3. In mathematical terms, Hamming codes are a class of binary linear codes. For each integer r≥2 there is a code with block length n=2^r-1 message length k=2^r-1. Hamming codes are used for parity generation. In this paper the authors considered only about the detection and correction of soft errors. These error detection and correction mechanisms are not dealing with isolated defects.

Haiso.M.Y in 1970[7] proposed a optimal minimum odd-weight column Single Error Correction and Double Error Detection (SEC-DED) code. This is similar to hamming SEC-DED code. Here the difference from the previous work is that, every column of H matrix contain odd number of ones and also all columns should be distinct. The minimum odd-weight column code is suitable for applications to computer memories or parallel systems. A computation indicates that this is better in performance, cost and reliability than are conventional Hamming single error correction and double error correction codes. Single-error-correction,double-error-detection codes (SEC-DED) are widely used to increase computer memory reliability.

The authors introduced some mechanisms to detect and correct soft errors during transmission for memory protection. But these introduced methods are not dealing with isolated defects. That is, in the presence of isolated defects, by using these methods there is no any way to detect and correct isolated defects. Costas Argyrides, Pedro Reviriego and Juan Antonio Maestro in 2013 proposed [4] an error correction code to protect against isolated defects and soft errors. This paper deals with the detection and correction of isolated defects in the presence of soft errors. All error detection and correction mechanisms depend on the parity bits. Here parity bits are generated by using hamming code. In this paper a new approach taken to deal with isolated defects. By using this new approach, it is possible to find out the presence of stuck at defects. Another problem with this existing method is the case that 1 defect (defect value stuck at bits opposite value) plus two soft errors will be miscorrected instead of showing that as double error. It provides better results compared to previous method. Modification to the existing error correction code is done based on this paper.

3. PROPOSED METHOD

The main problem when using SEC-DED correction to deal with manufacturing defects is that, when the word contain 1 defect (defect value stuck at bits opposite value) plus two soft errors will be miscorrected instead of showing that as double error. In this paper a new approach is introduced that deals with the case that, the word contain 1 defect (defect value stuck at bits opposite value) plus two soft errors, by using this new approach this case can be detected as double error instead of the word will be read miscorrected. Fig. 1. shows the case that the word contain one defect (defect value stuck at bits opposite value) plus two soft errors, Fig. 1. shows the situation for a word that suffers two soft errors and a defect. In this case the defect will not cause an error because the original data matches with the defects. But when reading the word an uncorrectable error is detected. This can be solved by using proposed method. In the proposed system, when a word suffers from two soft errors and a defect as illustrated in above figure (here the defect does not cause an error as the original data matches the stuck-at value), instead of detecting this as an uncorrectable error, the output will be indicate as double error.

**Fig. 1.** Word contain two soft errors and a defect

For achieving this new method additional registers are required. But the main problem associated with this proposed method to deal the case with word contain two soft errors and a defect (here the defect does not cause an error as the original data matches the stuck-at value) is that, due to the requirement of additional registers the
area of the encoder and decoder will increase to some extent. But in the case of 64 bit input data, it is possible to reduce the hardware area of encoder and decoder by using the proposed method (By reducing the number of ones in the each row and each column of H matrix). Fig.2. shows the block diagram of proposed method. The given block diagram shows the flow of proposed work.

This system is simulated by using XILINX ISE tool. Xilinx ISE (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. ModelSim is a widely used logic simulation tool for verification and debugging of digital circuits.

4. RESULTS AND COMPARISONS

The simulation output views of existing and proposed SEC-DED code is given. The proposed SEC-DED code circuit is also simulated and waveform obtained. The existing and proposed circuits are simulated by using the simulation tool “MODELSIM”. The design is coded by VHDL in XILINX 8.1 and simulated by MODELSIM 6.5f. The performance analysis compares existing and proposed error correcting circuit. And it shows the simulation output of the proposed system, when a word suffers from two soft errors and a defect (here the defect does not cause an error as the original data matches the stuck-at value), instead of detecting this as an uncorrectable error, the output will indicate as double error is given.

![Fig.3. Simulation output waveform of 64 bit data input encoder of the SEC-DED code](image1)

Fig.3. describes the output waveform of encoder output with 64 bit input data in the case of existing method. It shows the 72 bit encoded output data due to the generation of 8 bit parities.

![Fig.4. Output waveform of decoder where the input contain one defect (Defect value stuck at bit’s value) and two soft errors](image2)

Fig. 4. shows the simulation output of error correction code that contain 1 Defect (Defect value stuck at bit’s value) + 2 soft errors. Where defect1_0 indicate the presence of stuck at _0 and stuck at _1 defect. And i_defect indicate that in which position the error has occurred. If Double is 1 indicates the presence of double error. “Output” indicates the decoded output. Here soft errors occurred at the bit position two and three and stuck at defect occurred at bit position one of input. In this case the syndrome will mark a double error. The word will be copied into a register. Write all zeros to the word and read it back. Write all ones to the word and read it back. And locate the permanent error in the word. Change the value of that bit and re-evaluate the syndrome. The word will be miscorrected. This result is obviously a drawback of the existing technique.

![Fig.5. Output waveform of decoder where the input contain one defect (Defect value stuck at bit’s value) and two soft errors using proposed method](image3)

Fig.5. shows the simulation output of error correction code that contains 1 Defect (Defect value stuck at bit’s value) + 2 soft errors. Here soft errors occurred at the bit position two and three and stuck at defect occurred at bit position one of input. In this case the syndrome will mark a double error. The word will be copied into a register. Write all zeros to the word and read it back. Write all ones to the word and read it back. And locate the
permanent error in the word. Instead of changing permanent error the value of that bit copied from the input by using proposed method and re-evaluates the syndrome. The output will be detected as double error.

**CONCLUSIONS**

In this project, the use of SEC-DED to deal with both soft errors and isolated stuck-at defects has been studied. Then a technique has been proposed that can deal with both types of errors effectively by applying a modified error correction process. This approach would provide a complete approach to protect against defects and soft errors in memories. For a computer memory system with a specified word length, the number of check bits needed for an SEC code can be determined by the Hamming relationship. The modified SEC-DED code is capable of dealing the case with the case that 1 defect (defect value stuck at bits opposite value) plus two soft errors, by using proposed method this case can be detected as double error instead of the word will be read miscalculated. In this project, an effective technique to use ECC to deal with isolated defects and soft errors on memory chips is presented. A technique that can cope with either stuck-at-defects, soft errors, or both at the same time is illustrated. An efficient single error correction and double error detection code can deals with either stuck-at-defects, soft errors, or both at the same time. The aim of this work is to compare the existing Error Correcting Code with proposed method. This system is simulated by using XILINX ISE tool and the output simulated by MODELSIM 6.5f.

**REFERENCES**