

Design of Low-power and High Performance Pulse Triggered Flip-Flop

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ABSTRACT

In this paper a low power and low area pulse triggered flip flop has been analyzed. Power has become an important issue in modern Technology, especially for low power applications. The power consumed by clock is the dominant part in this VLSI Process Design. The flip-flop is the basic element of clocked signal and memory element. The idea in the proposed explicit type Pulse Triggered is to use one extra NMOS transistor to shorten the delay and power. The proposed design removes the long discharging problem and reduces D to Q delay. The proposed design is compared with some conventional designs i.e. $ieep$ -DCO, CDFP and MHLFF and the schematic and post-layout simulations have been done using GPDK 90nm VLSI technology in Cadence Virtuoso. The proposed design has resulted in reduction of overall power consumption up to 21%, 10.1% and 10.2% in comparison to some conventional technique $ieep$ -DCO, CDFP and HLFF respectively. The result also shows some reduction in leakage power

Index Terms – Flop-Flop, Pulse-triggered

1. INTRODUCTION

The power consumption in the electronic circuit and system is very important in modern VLSI Design [1]. The major fraction of the total power in modern synchronous system utilizing devices such as microprocessor is dissipated over the clock system. Latch and flip-flop are basic elements of clock in all kind of digital design. Nowadays pipelining technique are used in these digital design that employ flip-flop module such as first in first out register file. The 30% to 60% of the total power is consumed by clock distribution network and storage element. Hence flip-flop contributes a significant portion of chip area and power consumption to the overall system design [2]-[3].

Pulse triggered flip-flop is more popular due to its single latch structure than the conventional transmission gate and master-slave flip-flops in high speed operation [4]-[6]. Pulse triggered flip-flop consist a pulse generator for strobe signal and a latch for data storage. If the triggered pulse is sufficiently narrow then the latch work as edge triggered flip-flop. The conventional master-slave flip-flops are made up of two stages and they are characterized by hard edge triggered and thus consume larger area and power. Pulse triggered flip-flop leads to higher toggle rate for high speed operation.

Pulse triggered flip-flop can be categorized in two types. First one is implicit type and second one explicit type [7]. The classification is due to pulse generator. In implicit type flip-flop, the pulse generator is the part of flip-flop and in explicit type flip-flop the pulse generator is not a part of flip-flop. Explicit type flip-flop takes more power than implicit type but it has advantage that it can be share several flip-flop so overall power consumption is reduced. So for any system uses of explicit flip-flop will more energy efficient than using implicit flip-flop. That's why we will concentrate only on explicit flip-flop.

2. CONVENTIONAL EXPLICIT TYPE PULSE TRIGGERED FLIP-FLOP DESIGN

2.1 $ieep$ -DCO

$ieep$ -DCO is known as the explicit type Data Close to Output [7]. The schematic diagram of $ieep$ -DCO is shown in the fig. 1. It consists of NAND gate and inverter logic based pulse generator. The pulse width of pulse generator depends on delay of the three inverters. In the circuit inverter I3 and I4 is used to latch the data and I1 and I2 is used to hold the internal node. It has serious drawback, when the input data doesn't change then the internal node X charges and discharges at every clock cycle. Due to charging and discharging the switching power dissipation is larger and also glitches appeared at the output. To overcome this problem many other circuit developed like conditional discharge, conditional capture technique [8]-[11].

2.2 Conditional discharge flip-flop (CDFP) Design

The schematic diagram of conditional discharge flip-flop (CDFP) is shown in the fig. 2 [10]. It consist one extra NMOS transistor and the Q_{fbk} is connected to the input of this transistor. When the input Data is high than q_{fbk} is low so N1 is off so there is no discharging path at every clock cycle. Hence the switching power is reduced.

If the input changes from '0' to '1' the internal node X is discharge through N1, N2 and N3 assuming that (Q , Q_{fbk}) were initially (low, high). As the internal node X is discharged it pulled P2 ON and the output will be



charged. If the input switches from '1' to '0', then the first stage is disabled and node X retains its pre-charge state, and node Y will be high so the output Q is discharged through N4 and N5. Since node X is not charging and discharging periodically at every cycle no glitches will appear on the output node Q when the input Data stays high.

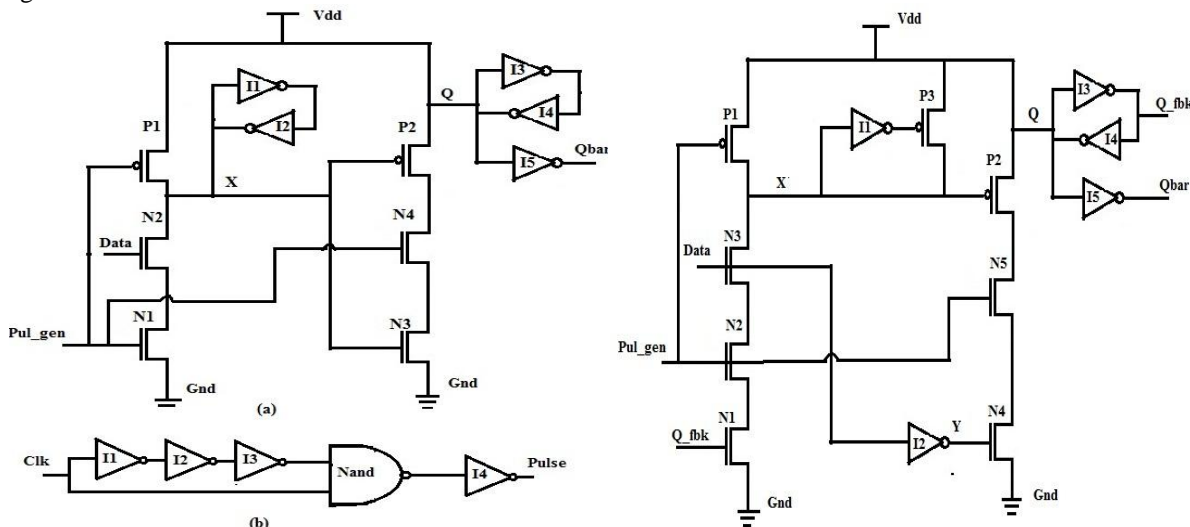


Fig. 1 Explicit type Data close to output pulse triggered flip-flop
 Fig. 2 Conditional discharge Flip-flop

2.2 MHLFF

MHLFF is known as modified hybrid latch flip-flop [12]. The schematic diagram of MHLFF shown is the fig 3. The MHLF is implicit type pulse triggered flip-flop. In this three inverter I1, I2, I3 and one NMOS is used to generate the pulse. Inverter I4 and I5 is used to latch the data in the output node Q. In this design, a weak pull-up PMOS P1 transistor used which is controlled by output signal Q. It is used to maintain the node level X at high when Q is zero. This design removes periodically discharging of node X. Hence, switching power reduced. But it takes longer Data to Q delay during '0' to '1' transition because node X is not precharge. Larger transistor N1 and N4 is required to enhance the discharging capability. Another drawback of this design that node X becomes floating when output Q and input data both equal to '1'.

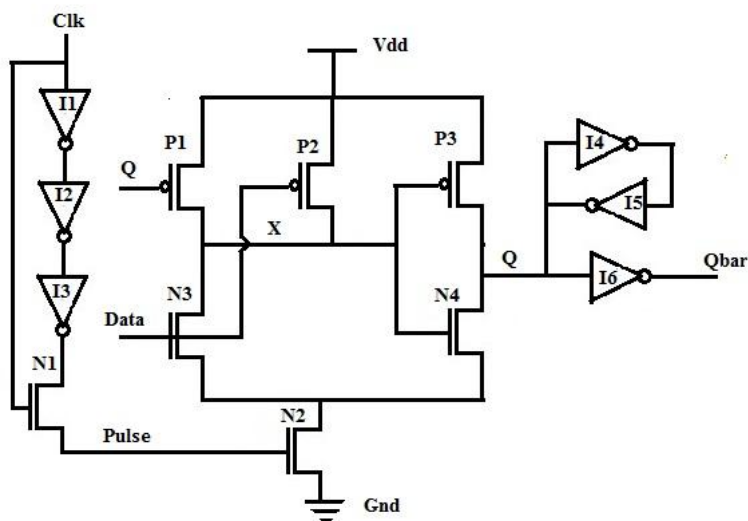


Fig. 3 Modified hybrid latch flip-flop

2.3 Modified pulse triggered Flip-Flop Design

Now we will compare these three conventional circuit with the proposed circuit. In these three circuits worst case occurs when data change from '0' to '1'. The idea in the proposed design is to use one extra NMOS. The proposed circuit has several advantages over earlier circuits. First, a weak pull-up PMOS transistor p1 is used so that the internal node X charges. The circuit act as pseudo-NMOS logic design and also it also reduces the load capacitance at node X [13]. Second a pass transistor Nx is used which is controlled by clock pulse. The input

data directly goes to the output Q so the Data to Q delay reduced. Third, the pull down network of the second stage is completely removed and pass transistor Nx provides a discharging path.

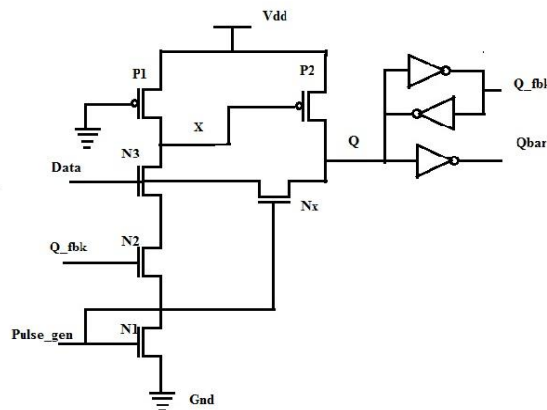


Fig.4 Schematic diagram of Modified Pulse Triggered Flip-Flop

The working principle of proposed design is as follows. When a pulse signal is applied to the input of the N1 and there is no change in the input data then the output will be same as input because of pass transistor Nx. The pass transistor transfers the signal to the Q without any delay. At that time input data and Q_fb are complement to each other so there is no discharging of node X. Now if the input switch from '0' to '1', the node X discharges to ground level through transistor N1, N2 and N3. When the node X discharges to ground level then P2 transistor becomes ON which pulls node Q to high. Due to this mechanism the delay is greatly reduced and also the node Q gets strong '1'. Now if the input switches from '1' to '0' the node X gets charge through weak PMOS transistor P1 and the node Q discharges through Nx. As the node discharges through Nx the output node Q will be strong '0'.

3. SIMULATION RESULTS

The simulation result for all conventional flip-flop and proposed were obtained by GPDK 90nm technology at room temperature using cadence virtuoso with 1.8 power supply and clocked frequency 500 Mhz. The simulation waveform of proposed design is shown in the fig 5. In the waveform we can see when the clock signal goes from '0' to '1' a pulse is generated. It means the flip-flop act as positive edge triggered. The design of pulse width is very crucial because if the pulse width is very small the data will not be captured and if the pulse width is long than power consumption will be high so the pulse width should be kept such that we get the optimize power consumption.



Fig. 5 Simulation waveform of Proposed Design

The characteristic comparisons of various flip-flop designs are summarized in the table I. From the table we can see that the number of transistors in the proposed design doesn't decrease but there is a significant decrease in the layout area. Also there is significant decrease in delay. To elaborate the power consumption behavior of these flip flop design we applied switching activity test patterns (100%, 50%, and 0%). From the test pattern, the proposed design is more power economical as compared to others. The power saving of proposed design against ep-DCO, CDFP and MHLFF are 21%, 10.1% and 10.2% respectively when the switching activity is 100%. The ep-DCO flip-flop consumes more power because when the data doesn't change at every clock. As the table

shows that there is decrease in power and delay in the proposed design there is significant decrease in power delay product as shown in fig 5.

The leakage power comparisons in standby mode of various flip-flop is summarized in table II. We applied four test patterns(0,0), (0,1), (1,0) and (1,1) by changing clk and data. The proposed design gives the minimized leakage power consumption which is mainly due to reduction in the transistor sizes along the discharge path.

TABLE I
Characteristic Comparison of Various Flip-Flop Designs Mode (μW)

Flip-Flop Design	ep-DCO	CDFP	MHLFF	Proposed
No. of transistor	28	30	19	24
Layout Area(μm^2)	71.43	74.6	58.93	58.71
Min Data to Q delay (pS)	127	132	146	123
Average Power(100% activity) μW	9.26	8.122	8.115	7.286
Average Power(50% activity) μW	8.632	7.9	7.447	7.075
Average Power(0% all 0) μW	8.104	6.306	6.839	6.255

TABLE II
Leakage Power Comparison in Standby

FF Design (Clk,Data)	Ep-DCO	CDFP	MHLFF	Proposed
(0,0)	4.81	3.66	2.398	2.65
(0,1)	3.123	2.38	2.4381	1.724
(1,0)	2.823	2.27	2.64	2.466
(1,1)	4.465	1.93	1.631	1.7

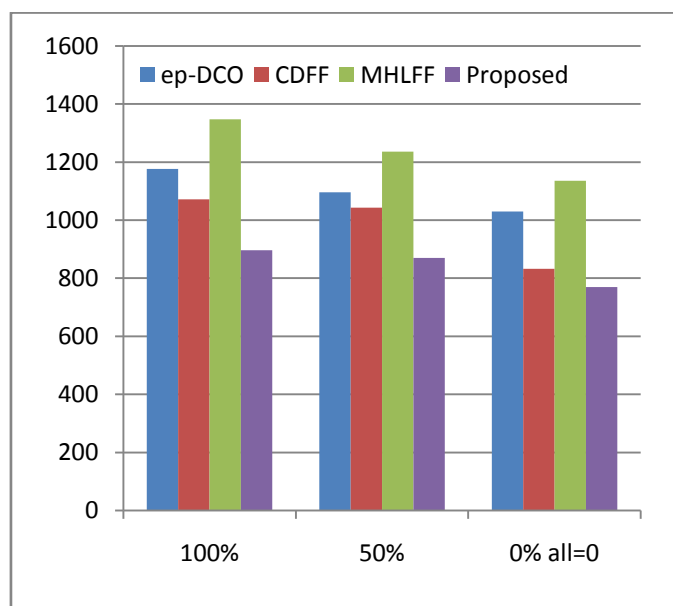


Fig.5 Power delay product performance under different switching activity

4. CONCLUSION

In this paper various flip-flop designs like ep-DCO, CDFF, MHLFF are discussed. The schematic and post layout simulation were done using GPDK 90nm technology in cadence virtuoso. The idea in the proposed design is to add one extra NMOS to shorten the delay and area. The overall power consumption of proposed design reduced up to 21%, 10.1 and 10.2% with respect to ep-DCO, CDFF and MHLFF respectively. The D to Q delay of proposed FF is reduced by 15.75%, 6.8% & 3.14% with respect to MHLFF, CDFF, ep-DCO respectively. The layout areas of proposed FF is also reduced by 0.37%, 21.3% & 17.80% with respect to MHLFF, CDFF, ep-DCO respectively even after the increase in number of transistors. In the proposed design there is a little bit reduction in leakage power also. Hence the overall performance of the flip-flop is enhanced.

REFERENCES

- [1]. KIAT-SENG Y, ROFAIL S, GOH W L. CMOS/BiCMOS ULSI: Low voltage, low power [M]. Singapore: Prentice Hall, 2002: 1–11.
- [2]. H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid-State Circuits*, vol. 33, pp. 807–811, May 1998.
- [3]. K. Chen, "A 77% energy saving 22-transistor single phase clocking Dflip-flop with adoptive-coupling configuration in 40 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Nov. 2011, pp. 338–339.
- [4]. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high speed sense-amplifier-based flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 11, pp. 1266–1274, Nov. 2005.
- [5]. H. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *IEEE Tech. Dig. ISSCC*, 1996, pp. 138–139.
- [6]. F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R. Wang, A. Mehta, R. Heald, and G. Yee, "A new family of semi-dynamic and dynamic flip flops with embedded logic for high performance processors," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 712–716, May 1999.
- [7]. J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high performance microprocessors," in *Proc. ISPLED*, 2001, pp. 207–212.
- [8]. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.
- [9]. N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power-efficient dual-edge clocking," in *Proc. Int. Symp. Low-Power Electron. Design*, Aug. 2002, pp. 56–59.
- [10]. P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low power conditional discharge flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 477–484, May 2004.
- [11]. Y.-T. Hwang, J.-F. Lin, and M.-H. Sheu, "Low power pulsetriggered flip-flop design with conditional pulse enhancement scheme," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 2, pp. 361–366, Feb. 2012.
- [12]. S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani, "Low power single- and double-edge-triggered flip-flops for high speed applications," *IEE Proc. Circuits Devices Syst.*, vol. 152, no. 2, pp. 118–122, Apr. 2005.
- [13]. H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra low power clocking scheme using energy recovery and clock gating," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 1, pp. 33–44, Jan. 2009.
- [14]. P. Zhao, J. McNeely, S. Venigalla, G. P. Kumar, M. Bayoumi, N. Wang, and L. Downey, "Clocked-pseudo-NMOS flip-flops for level conversion in dual supply systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 9, pp. 1196–1202, Sep. 2009.
- [15]. Yin-Tsung Hwang, Jin-Fa Lin, and Ming-Hwa Sheu, "Low-Power Pulse-Triggered Flip-Flop Design With Conditional Pulse-Enhancement Scheme" *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*, VOL. 20, NO. 2, FEBRUARY 2012

