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DESIGN OF HIGH SPEED AND AREA EFFICIENT UNSIGNED MULTIPLIER USING CBL TECHNIQUE

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ABSTRACT

This project deals with the comparison of the VLSI design of the conventional SQRT Carry Select Adder (SQRT CSLA) based unsigned integer multiplier and the VLSI design of the Modified Carry Select Adder (MCSLA) based unsigned integer multiplier. Both the VLSI design of multiplier multiplies two 32-bit unsigned integer values and gives a product term of 64-bit value. The MCSLA based multiplier delay time reduced to nearly 13 % for performing multiplication operation by conventional SQRT CSLA based multiplier. And also the area needed for MCSLA based multiplier is reduced to nearly 44.6 % by the conventional SQRT CSLA based multiplier to complete the multiplication operation. These multipliers are designed by Verilog HDL and synthesized by using Xilinx 14.6 for Spartan 3E FPGA kit and timing diagrams are viewed through I Sim simulator.

Keywords: *SQRT CSLA, MCSLA, Delay, Area, Verilog Modeling & Simulation.*

1. INTRODUCTION

Digital computer arithmetic is an area of logic design with the objective of developing appropriate algorithms in order to provide high speed and efficient utilization of the available hardware. The basic operations in digital computer arithmetic are addition, subtraction, multiplication and division. In this, we are going to deal with the process of additions implemented to the operation of multiplication. The repeated form of the addition operations followed by shifting results in the multiplication operations. In VLSI designs, chip area, power and delay are the most important measures for determining the performance and efficiency of the VLSI architecture. Additions and multiplications are most widely used arithmetic operations performed in all digital signal processing applications like FFT, FIR and IIR. Addition is a fundamental operation for any digital multiplication. An area efficient high speed and accurate operation of a digital system is greatly influenced by the performance of the used adders. In this project we are going to compare the performance of different adder based multipliers under consideration of area and time needed for calculation. On comparison with the SQRT CSLA based multiplier the area of calculation of the MCSLA based multiplier is smaller and also the delay time reduced. Here we are dealing with the two 32 bit input (n*n) and resultant 64 bit (2n) output.

2. CONVENTIONAL SQRT CARRY SELECT ADDER

The conventional Square Root Carry Select Adder is having dual Ripple Carry Adder with 2:1 multiplexer for each section of Sum and Carry. The major disadvantage of conventional SQRT CSLA is the large area requirement because of multiple pairs of Ripple Carry Adder. The Conventional 16-bit SQRT Carry Select Adder is shown in Fig.1.

It is divided into five sections with different bit size ripple carry adder. From the design of conventional SQRT CSLA, there is scope for reducing delay and area requirement.

In conventional SQRT CSLA, both Sum and Carry bits are calculated for two alternatives that is carry input Cin= O and Cin= 1. Once Cin is delivered from previous stage, the correct computation is chosen using a mux to produce the exact output. Instead of waiting for Cin to calculate the sum, the sum is correctly taken at output as soon as Cin gets there.

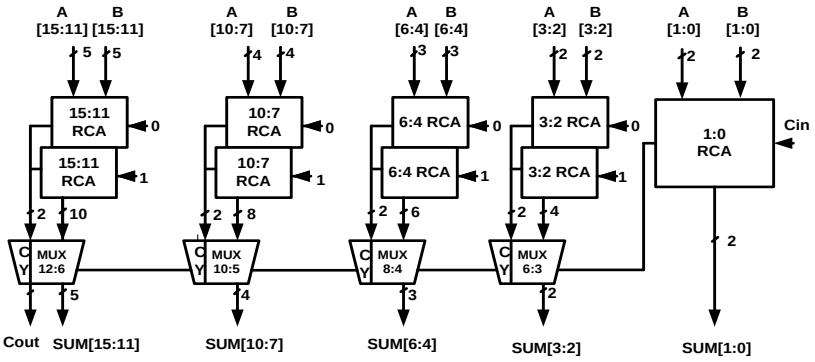

Fig.1 Conventional 16 bit SQRT CSLA

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3. COMMON BOOLEAN LOGIC

Analyzing the truth table of a single bit full adder shown in Table 1, One can observe, to find out the output of summation signal, as carry input signal Cin= 0, is done by taking EX-OR of given two input and carry is obtain by taking AND operation of two input signal. Similarly if carry input signal is Cin= 1 summation is inverse of EX-OR that is Ex-NOR of two input and carry is OR operation of two input signals.
By sharing the Common Boolean Logic concept an efficient adder can be design.

Table 1. Truth Table of Single bit Full Adder

C_{in}	A	B	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4. PROPOSED ARCHITECTURE

In proposed architecture, an area efficient and improved delay performance Modified Carry Select Adder is designed. This is done by sharing the Common Boolean Logic concept to remove the paired adder cells in conventional carry select adder. In this way, it save many logic gate counts resulting less area requirement and improved delay performance.

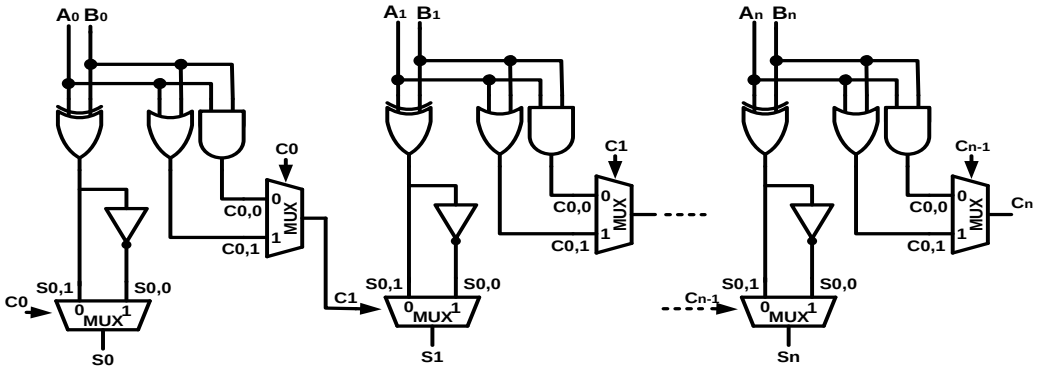

Fig.2 CBL based adder architecture

By using the Common Boolean Logic term in summation generation, a proposed Modified Carry Select Adder design is shown in Fig.2. To utilize the Common Boolean Logic term for summation, it only needs to implement one XOR gate and one Inverter. And for Carry calculation one OR gate and one AND gate. And to get the desired output 2:1 Mux is used. Depending on the carry-in signal 2:1 Mux gives output.

5. MULTIPLICATION PROCESS OF UNSIGNED DATA

In multiplication process partial product generates that is one for each digit in the multiplier. And to produce the final product these partial products are summed. The multiplication process of two n-bit binary integers results in a product of up to 2n bits in length. The process of multiplication can be understand in following steps,
1: Multiplier and multiplicand are stored in two (n) 32-bit registers a and b.
2: A third register c is generated of (2n) 64-bit having initial value as '0'.
3: Each bit of multiplier is multiplied to the multiplicand followed by shifting result one bit to the left.
4: At final stage these results are added to get the final result in register c.
This process of multiplication is shown in Fig.3.

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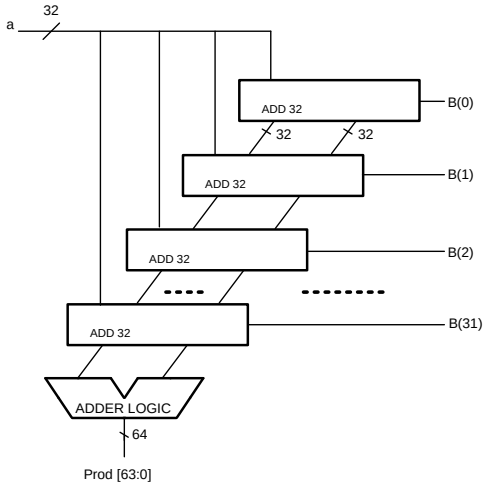

Fig.3 Schematic of multiplication process

6. VERILOG SIMULATION

The Verilog simulation result of the two multipliers is shown in this section. In this part, timing diagrams, waveforms and the design summary for both the SQRT CSLA and MCSLA based multipliers are shown in the figures. The Verilog HDL code for both multipliers, using SQRT CSLA and MCSLA, are generated. The Verilog HDL model has been developed using Xilinx 14.6 for Spartan 3E FPGA kit and simulation results are viewed through I Sim simulator. The multipliers use two 32-bit input values and give 64-bit output.

Fig.4 and Fig.5 shows the input given to the multiplier and resultant output. The timing diagram shows that result is same in both multipliers for same input values. The synthesized report for area estimation is shown in Fig.6 and Fig.7. From the report it is clearly visible the total number of Look Up Table required in SQRT CSLA based multiplier and MCSLA based multiplier.

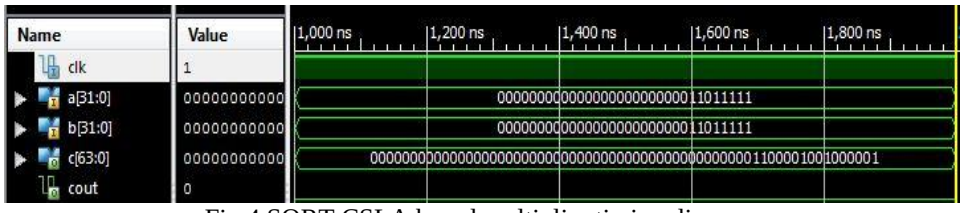

Fig.4 SQRT CSLA based multiplier timing diagram

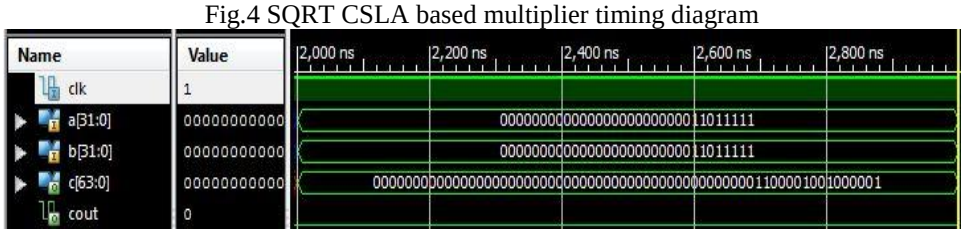

Fig.5 MCSA based multiplier timing diagram

mul32 Project Status (05/31/2014 - 08:52:22)			
Project File:	Project.xise	**Parser Errors:**	No Errors
Module Name:	mul32	**Implementation State:**	Placed and Routed
Target Device:	xc3s1600e-5fg320	**•Errors:**	
Product Version:	ISE 14.6	**•Warnings:**	
Design Goal:	Balanced	**•Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	
Environment:	System Settings	**•Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	3,693	29,504	12%	
Number of occupied Slices	1,964	14,752	13%	
Number of Slices containing only related logic	1,964	1,964	100%	
Number of Slices containing unrelated logic	0	1,964	0%	
Total Number of 4 input LUTs	3,693	29,504	12%	
Number of bonded IOBs	129	250	51%	
Average Fanout of Non-Clock Nets	4.74			

Fig.4 SQRT CSLA based multiplier synthesis report.

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mul32 Project Status (05/31/2014 - 09:03:36)			
Project File:	Project.xise	**Parser Errors:**	No Errors
Module Name:	mul_mcsa32	**Implementation State:**	Placed and Routed
Target Device:	xc3s1600e-5fg320	**•Errors:**	No Errors
Product Version:	ISE 14.6	**•Warnings:**	
Design Goal:	Balanced	**•Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	
Environment:	System Settings	**•Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	2,046	29,504	6%	
Number of occupied Slices	1,027	14,752	6%	
Number of Slices containing only related logic	1,027	1,027	100%	
Number of Slices containing unrelated logic	0	1,027	0%	
Total Number of 4 input LUTs	2,046	29,504	6%	
Number of bonded IOBs	129	250	51%	
Average Fanout of Non-Clock Nets	3.82			

Fig.5 MCSA based multiplier synthesis report

7. PERFORMANCE ANALYSIS

Performances in terms of different parameters are calculated for conventional design and proposed design. And they are compared. These results are shown below.

7.1 Area Analysis

The performance analysis for the area of SQRT CSLA and MCSLA based multipliers in terms of number of Look Up Table (LUT) required is represented in the form of the diagram shown in Fig.8.

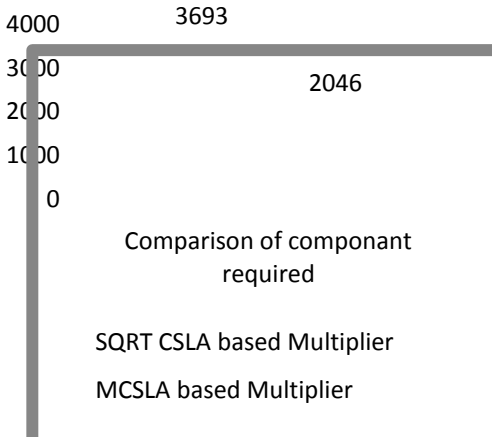

Fig.8 Area analysis

7.2 Delay Analysis

The performance analysis for the delay of SQRT CSLA and MCSLA based multipliers in nanoseconds is represented in the form of the diagram shown in Fig.9.

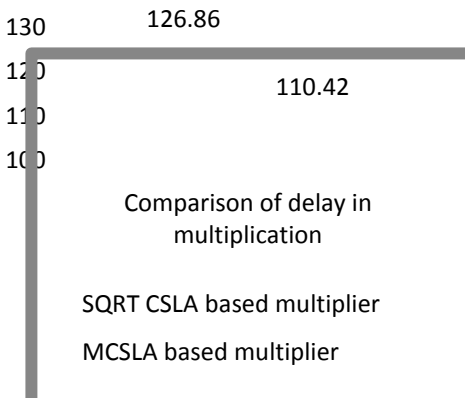

Fig.9 Delay analysis

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7.3 Area Delay Product

The performance analysis for the area delay product of SQRT CSLA and MCSLA based multipliers is represented in the form of the diagram shown in Fig.10.

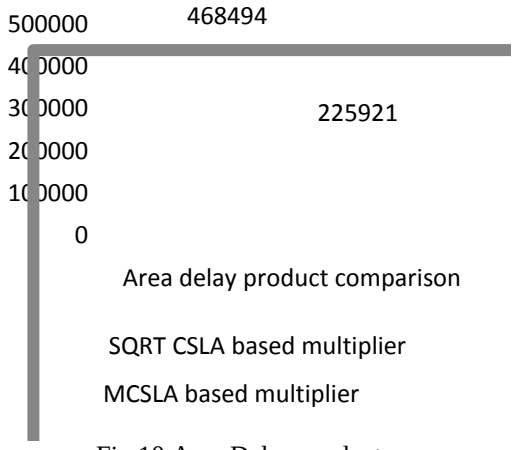

Fig.10 Area Delay product

7.4 Analysis Table

Analysis table for final result is shown in Table 2.

Table.2 Result analysis

Type of multiplier	Area(LUT)	Delay(ns)	Delay area product
SQRT CSLA based	3693	126.86	468494
MCSLA based	2046	110.42	225921

8. CONCLUSION

The design of a 32-bit unsigned multiplier with SQRT CSLA and MCSLA was presented. Verilog HDL was used to model the system on Xilinx 14.6 tool for Spartan 3E FPGA kit and timing waveform seen with the help of ISim. From synthesized report analysis it is clearly visible that by using MCSLA based multiplier Area, Delay and overall performance that is area delay product improved as compared to Conventional SQRT CSLA based multiplier. The improvement in area requirement is about 44.6 % in terms of LUT used and in delay performance it is about 13% hence the proposed design is better than the previous one.

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