Vol 05, Article 09411, September 2014
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

A NOVEL ARCHITECTURE FOR MAC UNIT USING REVERSIBLE LOGIC GATES

R. SIVA SAI[1], C.LEELA MOHAN[2], M.SREELAKSHMI[3]
[1]PG-Student, VLSI, [2]Assosiate Professor, ECE Department, NEC, Nellore, Andhra Pradesh, INDIA
[3]Assistant Professor, ECE Department, CREC, Tirupati, Andhra Pradesh, INDIA
[1]sivasai494@gmail.com, [2]leelamohan416@gmail.com, [3]oohadwaraka@gmail.com

ABSTRACT

Hardware and timing complexities of MAC unit to perform arithmetic operation like addition or multiplication especially in the field of Digital Signal Processing (DSP) are the major issues to the designer. Here a new compensation method that reduces both the hardware and timing complexities of the multiplier used for DSP application has been proposed. The main aim of the proposed system is to design a MAC unit using reversible logic with least number of gates, number of garbage outputs, delay and quantum cost in order to prove it as an efficient design. For irreversible circuits, loosing one bit of information dissipates (kTln2) joules of heat energy, where k is Boltzmann's constant and T is the absolute temperature. The reversible circuits do not dissipate energy as much as irreversible circuits. Thus, energy dissipation is proportional to the number of bits lost during computation.

Keywords: *MAC Architecture, Reversible logic gates.*

1. INTRODUCTION

Reversible processing is a design of processing where the computational procedure at some level is reversible, i.e., time-invertible. A necessary situation for reversibility of a computational design is that the conversion function applying declares to their successors at a given later time should be one-to-one. Reversible processing is usually regarded an non-traditional form of processing. There are two significant, closely-related, kinds of reversibility that are of particular attention for this purpose: physical reversibility and logical reversibility. A procedure is said to be physically reversible if it outcomes in no improve in actual entropy; it is isentropic.

In almost all DSP programs the crucial functions are the multiplication and accumulation. Real-time signal processing needs high-speed and great throughput Multiplier-Accumulator (MAC) device that takes in low energy, which is always a key to accomplish a top rated digital processing system. The objective of this work is, design and execution of a low energy MAC device with prevent allowing strategy to save energy. First of all, a 1-bit MAC device is designed, with appropriate geometries that give enhanced energy, area and delay. The delay in the pipeline levels in the MAC device is approximated depending on which a management device is designed to management the information dataflow between the MAC prevents for low energy. In the same way, the N-bit MAC device is designed and managed for low energy using a management reasoning that allows the pipelined levels at appropriate time. The adder cell designed has benefits of great operational speed, small gate count and low energy.

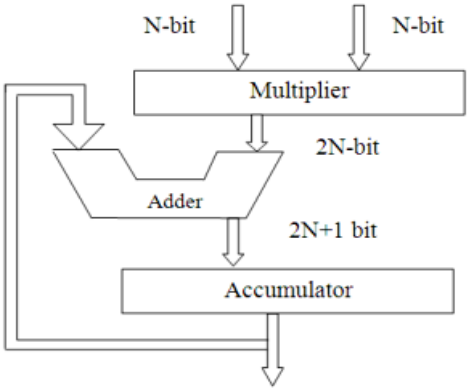

Fig-1: Basic MAC diagram

In common, a multiplier uses Booth's algorithm and range of full adders (FAs), or Wallace tree instead of the range of FA's., i.e., this multiplier mainly includes the three parts: Booth encoder, a shrub to compress the partial products such as Wallace tree, and last adder . Because Wallace shrub is to add the partial products from encoder as similar as possible, its function time is proportionate to, where is the variety of information. It uses the fact that keeping track of the variety of 1's among the information decreases the variety of results into. In actual implementation, many (3:2) or (7:3) surfaces are used to decrease the variety of results in each direction step. The most effective way to improve the rate of a multiplier is to decrease the variety of the partial products because multiplication continues a sequence of additions for the partial products. To decrease the variety of

Vol 05, Article 09411, September 2014
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

computation actions for the partial products, MBA algorithm has been used mostly where Wallace shrub has taken the part of improving the speed to add the partial products. To improve the rate of the MBA algorithm, many parallel multiplication architectures have been investigated.
A multiplier can be separated into three functional actions. The first is radix-2 booth encoding in which a partial product is created from the multiplicand X and the multiplier Y. The second is adder array or partial product compression to add all partial products and convert them into the way of sum and carry. The last is the final addition in which the ultimate multiplication outcome is created by including the sum and the carry. If the procedure to obtain the increased outcomes is involved, a MAC comprises of four actions, as proven in Fig. 1, which reveals the functional actions clearly.
A common hardware structure of this MAC is proven in Fig. 2. It carries out the multiplication function by multiplying the input multiplier X and the multiplicand Y . This is added to the past multiplication outcome Z as the accumulation step.
The N-bit 2's complement binary number can be expressed as

$$X = -2^{N-1}x_{N-1} + \sum_{i=0}^{N-2} x_i 2^i, \qquad x_i \in 0,1.$$

.....(1)

If (1) is expressed in base-4 type redundant sign digit form in order to apply the radix-2 Booth's algorithm.

$$X = \sum_{i=0}^{N/2-1} d_i 4_i$$

$$d_i = -2x_{2i+1} + x_{2i} + x_{2i-1}.$$

.....(2)

If (2) is used, multiplication can be expressed as

$$X \times Y = \sum_{i=0}^{N/2-1} d_i 2^{2i} Y.$$

……(3)

If these equations are used, the afore-mentioned multiplication–accumulation results can be expressed as

$$P = X \times Y + Z = \sum_{i=0}^{N/2-1} d_i 2^i Y + \sum_{j=0}^{2N-1} z_i 2^i.$$

…….....(4)

Each of the two conditions on the right-hand side of (4) is measured individually and the outcome is created by including the two outcomes. The MAC structure applied by (4) is known as the conventional style.

2. PROBLEM STATEMENT

For irreversible circuits, losing one bit of details reduces (kTln2) joules of heat energy, where k is Boltzmann's continuous and T is the absolute temperature. The irreversible circuits do not dissipate energy as much as irreversible circuits. Thus, energy dissipation is proportionate to the variety of bits lost during calculations. The irreversible circuits do not lose information and can generate unique results from specified inputs and vice versa (there is a one-to-one mapping between inputs and outputs). To experience low energy designs Huge processing and irreversible circuits are used. 1.3 Aim In the majority of DSP applications the critical functions are the multiplication and accumulation. Real-time indication handling requires high-speed and great throughput Multiplier-Accumulator (MAC) device that takes in low energy, which is always a key to accomplish a top rated DSP program. The main aim of the suggested program is to emphasize an efficient design of a irreversible MAC device to be able to prove that new routine outperforms the previously suggested one in terms of variety of gateways, variety of rubbish results, delay and quantum cost.

3. PROPOSED SYSTEM

In the majority of electronic indication handling (DSP) programs the crucial functions usually include many multiplications and/or accumulations. For real-time indication handling, a high-speed and great throughput Multiplier-Accumulator (MAC) is always a key to accomplish a top rated electronic indication handling program. In the last few years, the main consideration of MAC style is to improve its rate. This is because, rate and throughput rate is always the issue of electronic indication handling program. Pipelined multiplier / accumulator architectures and routine style techniques which are appropriate for applying great throughput indication handling methods and simultaneously accomplish low power intake. A traditional MAC unit includes

Vol 05, Article 09411, September 2014 International Journal of VLSI and Embedded Systems-IJVES
http://ijves.com ISSN: 2249 – 6556

(fast multiplier) multiplier and an accumulator that contains the sum of the past successive products. The operate of the MAC unit is given by the following equation:

$F = \Sigma A i Bi$

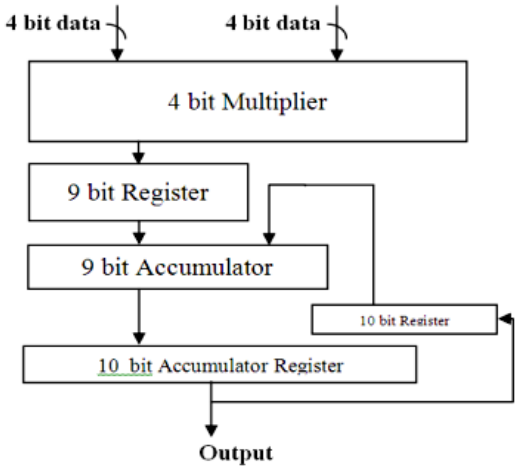

Fig-2: MAC architecture

The primary objective of a DSP processer style is to improve the rate of the MAC device, and simultaneously period restrict the energy intake. In a pipelined MAC routine, the wait of direction level is the wait of a 1-bit complete adder (Jou, Chen, and Su, 1995). Calculating this wait will support in determining the overall wait of the pipelined MAC. In this perform, 1-bit complete adder is developed. Place, energy and wait are measured for the complete adder, depending on which the pipelined MAC device is developed for low energy.

3.1 Design of Reversible Multiplier

The proposed reversible multiplier is designed in two phases.

Part I: Partial Product Generation (PPG)

Part II: Multi-Operand Addition (MOA)

The function of a 4*4 reversible multiplier is proven in Determine 15. It includes 16 Limited product pieces of the X and Y information to execute 4 * 4 multiplications. However, it can be prolonged to any other n * n reversible multiplier. In this we style a multiplier using reversible gateways. The reversible gateways used in the style of multiplier are Peres checkpoint and Peres complete adder checkpoint.

Fig-3: Partial Product Generation

Partial items can be produced in similar using 16 Peres gateways as proven in Determine 16.

Thisuses 16 Peres gateways and is a better routine as it has less components complexness and huge price in comparison to other gateways. An essential factor that should be regarded is that in an n×n similar multiplier (in undoable logic) for producing partial items in similar, n duplicates of each bit of the operands are required. Therefore, some fan-out gateways are required. The variety of fan-out gateways required for the undoable 4×4 multiplier is 24

3.2 Reversible multiplier and accumulator circuit

The function of the 4x4 multiplier is portrayed in Determine 2.4. It includes 16 partial product pieces of the type xi.yi. The undoable 4x4 multiplier routine has two areas. First, the partial items are produced in similar using Peres gateways proven in Determine 2.3. Then, the inclusion is conducted. The Partial Product generation circuit using Peres gateways primary mobile for such a multiplier is a Complete Adder (FA) recognizing three pieces and one continuous feedback. We use PFAG checkpoint as undoable full adder. The suggested undoable multiplier routine uses eight undoable PFAG full adders. Moreover, it needs four undoable 50 percent adders. It is possible to use PFAG checkpoint as 50 percent adder as said before in this research, but we use Peres checkpoint as undoable 50 percent adder because it has less components complexness and huge price as opposed to PFAG checkpoint (quantum price of Peres checkpoint is 4 whereas for PFAG it is 8).

Vol 05, Article 09411, September 2014
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

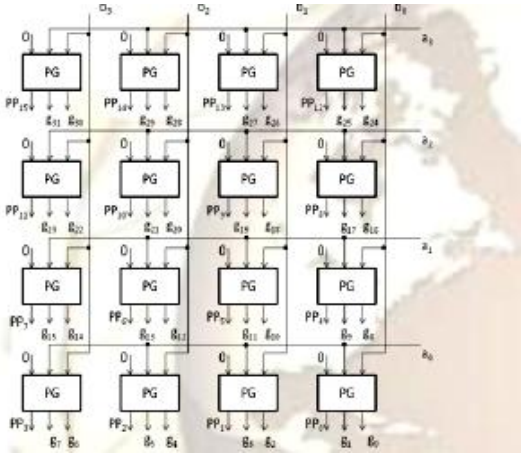

Fig-4: Partial product generation using peres gates

3.3 Accumulator unit

The routine of determine 15 using the peres gateways is a bit-wise multiplier which produces the limited items PP0 to PP15 for a 4x4 multiplication and these limited items will be provided to the multiplier routine proven in determine 16. The multiplier's development idea is proven in determine 17 which designed depending on multiplication proven in determine 14. The routine of determine 16 (using FA, HA) uses 4 Half adders and 8 Complete adders. The routine of the multiplier is actually an adder generating the 8-bit item outcome P0 to P7.

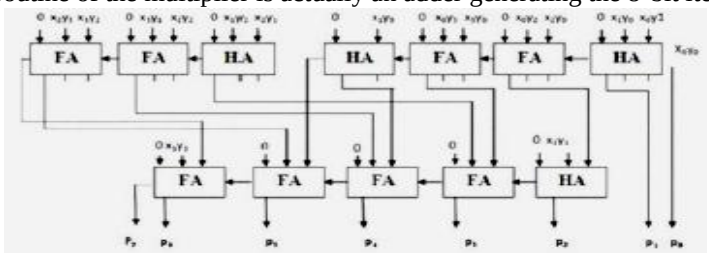

Fig-5: The concept of product generation

The accumulator and buffer both are as shown in figure 4.6. This circuit is constructed using the HNG, PG and FG gates. HNG gate is used as full adder to serve as the accumulator and the FG gates are used to serve as the buffer circuits. Each HNG gate produces 2 garbage outputs since we have not used the two outputs P & Q as shown in figure 19.

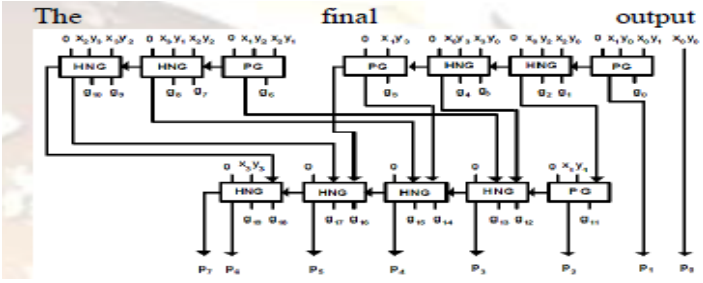

Fig-6: carry generation with help of HNG and Peres gates

It contains 9 bits including the carry generated during accumulation. The role of the FG gate is to serve as the buffer which can be cleared referring the figure 20 first input(A) of FG gate is SUM output og the HNG gate which will be brought out unchanged since the other input of the gate is made '0'. The other output, which is A is fed back to the HNG gate to serve as the prevous output. The FG gate is used here since there is no fanout in reversible logic. Furthur, it does not produce any garbage outputs.

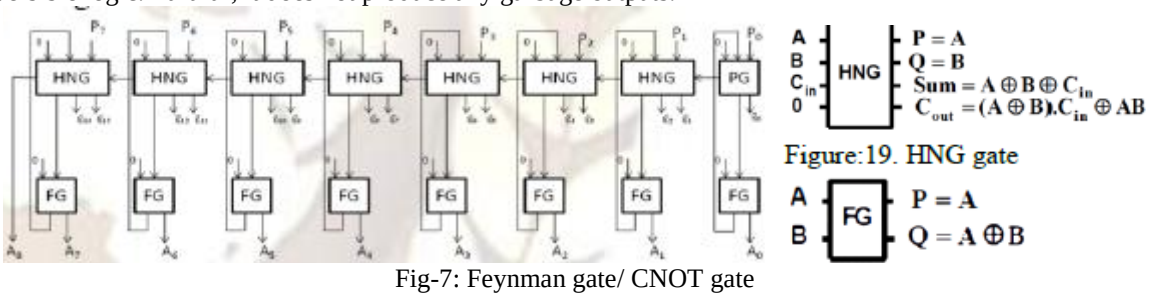

Fig-7: Feynman gate/ CNOT gate

Vol 05, Article 09411, September 2014
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

4. SIMULATION AND RESULT

The waveform shown below is the simulation results for PG GATE. Here the PG GATE having 3 inputs named as A, B & C and the ouputs are named as P, Q & R. The simulation results for PG GATE are observed by taking all combinations of the inputs. The outputs verified with reference to the PG GATE definition.

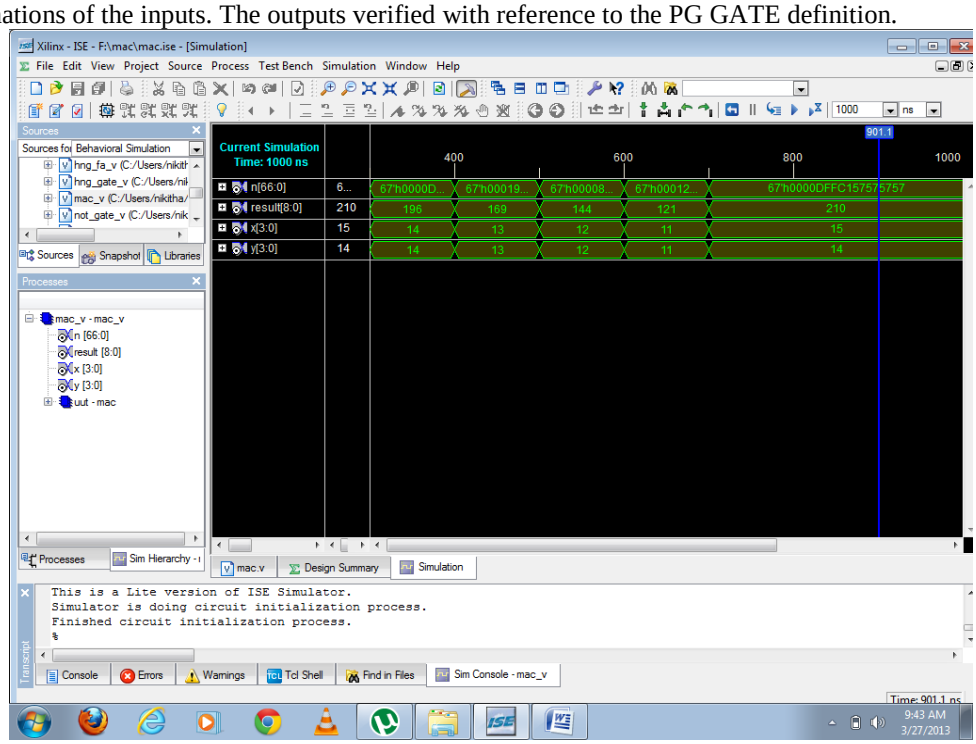

Fig-8: simulation result

COMPARISION TABLE

Rdix-2 MBA	No of LUTs	Slices
Radix-2 Conventional Logic Gates	184	397
Radix-2 Reversible Logic Gates	49	28

5. CONCLUSION

In this paper we can state that our design approach is better than all the existing designs in terms of number of constant inputs. Comparing our proposed reversible multiplier circuit with the existing circuits in , it is found that the proposed design approach requires 28 reversible logic gates but the existing design in requires 40 reversible gates and the existing design also requires 29 reversible gates, Furthermore, the restrictions of reversible circuits were highly avoided.

REFERENCES

[1]. Landauer, R., 1961. Irreversibility and heat generation in the computing process, IBM J. Research and Development, 5 (3): 183-191.
[2]. Bennett, C.H., 1973. Logical reversibility of computation, IBM J. Research and Development, 17: 525-532.
[3]. Kerntopf, P., M.A. Perkowski and M.H.A. Khan, 2004. On universality of general reversible multiple valued logic gates, IEEE Proceeding of the 34th international symposium on multiple valued logic (ISMVL'04), pp: 68-73.
[4]. Banerjee A., Pathak A., Optically implementable plans of reversible consecutive gadgets, Ind. J. Phys., vol. 8, pp. 1063-1068, Sept. 2010.
[5]. Banerjee A., Pathak A., Probabilistic Model of Fault Detection in Quantum Circuits Lect. Notes Phys., vol. 802, pp. 297_304, 2010.
[6]. Banerjee A., Pathak A., An calculation for minimization of quantum cost_ , Appl. Math Info. Sc., 2010, in press.
[7]. Banerjee A., Pathak A., Reversible Multiplier Design_ , International Conference on Emerging Trends in Engineering and Technology ICETET 2010, BITS, Goa, India, Nov. 2010.
[8]. Pathak A., Banerjee A., efficient quantum circuits for flawless and controlled teleportation of n-qubit non-maximally ensnared states of summed up Bell-type, Int.j. Quant.inf., 2010, in press.
[9]. Banerjee A., Pathak A., Comment on Quantum teleportation through GHZ-like state_ , Int.j. Theo. Phy., doi:10.1007/s10773-010-0561-5.