

A MULTIBAND FLEXIBLE INTEGER-N DIVIDER BASED ON PULSE SWALLOW TOPOLOGY

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ABSTRACT

The clock distribution network consumes approximately 70% of the total power which is dissipated by the ICs since it is the only indicator has the most switching activity. Typically we create a multiple PLL to meet the need, for a multi clock domain network, this project main aim is to develop a low power single clock multiband system which will supply for the multi clock domain system. This is highly recommended in wireless communication applications like Bluetooth, Zigbee. WLAN frequency synthesizers are designed based on pulse-swallow topology and the proposed are modeled using Verilog simulation using Modelsim and is implemented in Xilinx.

Keywords: : Phase Locked Loop (PLL), WLAN, pulse swallow topology

1. INTRODUCTION

Wireless LAN (WLAN) in the multi gigahertz bands such as HYPERLAN II and IEEE 802.11 a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like IEEE802.15.4 are recognized for low-rate data transmissions. The best published frequency synthesizer at 5 GHz consumes 9.7milliWatt IV supply, where its complete divider consumes power around 6mW, where the first stage divider is implemented using the source-coupled logic (SCL) circuit which allows higher operating frequencies but uses more power. The divider also uses an improved low-power loadable bit-cell for the Swallow S counter. The frequency synthesizer is one of the basic building blocks in modern communication systems. The operating frequency of the frequency synthesizer is limited by the frequency divider and the voltage-controlled oscillator. The function of channel selection in the frequency synthesizer demands programmable division ratios for the frequency divider.

The integer-N frequency synthesizer is more practical, less costly and of low spurious sideband performance as compared with the fractional-N frequency synthesizer. It is usually formed by a prescaler, a program counter (P counter) and a swallow counter(S counter). Such a topology can provide a programmable division ratio of $N \times P + S$, where N, P and S are the division ratios of three blocks respectively. The prescaler provides a dualmodulus of $N=N+1$. The P counter provides a fixed division ratio according to the requirement of the overall division ratio, while the continuous division ratios from 3 to $2n$ is achieved through the S counter by periodically reloading the divide-by-2 stages, where n is the number of stages of the S counter. Much research has been focused on the prescaler design for its highest operating frequency.

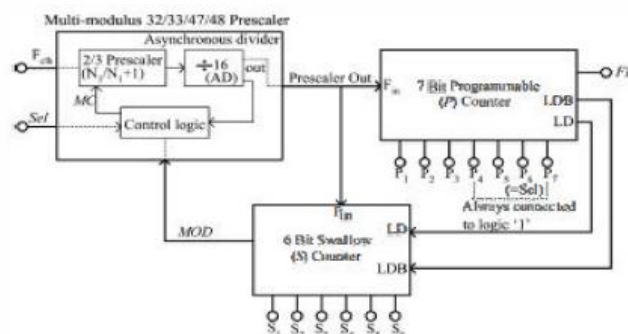


Fig.1. Proposed dynamic logic multiband flexible Divider

To satisfy these requirements, different reference frequencies, and different arrangement for N, P and S counters are selected for different applications. For example, only the UNII bands are covered. In this paper, a new wide-band high resolution programmable frequency divider is proposed. The wide band and high resolution are obtained by using the all-stage programmable topology in both counters. The high-speed frequency divider is a key block in frequency synthesis. The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input frequency. A dual-modulus prescaler usually consists of a divide-by-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units. The operation of the divide-by-2/3 unit at the highest input frequency makes it the bottleneck of the prescaler design. To achieve the two different division ratios, D flip-flops (DFFs) and additional logic gates, which reduce the operating frequency by introducing an additional propagation delay, are used in the unit. The power consumption of this divide-by-

2/3unit, which is the greatest portion of the total power consumption in the prescaler, significantly increases due to the power consumption of the additional components.

2. METHODOLOGIES

The power consumption and operating frequency of the extended true single-phase clock (E-TSPC)-based frequency divider is investigated. The short-circuit power and the switching power in the E-TSPC-based divider are calculated and simulated. A low-power divide-by-2/3 unit of a prescaler is proposed and implemented using a CMOS technology. Compared with the existing design, a 25% reduction of power consumption is achieved. A divide-by-8/9 dual-modulus prescaler implemented with this divide-by-2/3 unit using a 0.18- μm CMOS process is capable of operating up to 4 GHz with a low-power consumption. The prescaler is implemented in low-power high-resolution frequency dividers for wireless local area network applications. A new divide-by-2/3 unit with low power consumption has been proposed. It is suitable for the high-speed CMOS prescaler design. A divide-by-8/9 dual-modulus prescaler implemented with the proposed unit has been implemented to achieve the ultra-low-power consumption.

The dual-modulus operation above 4 GHz in the TSPC-based prescaler has first been achieved. The prescaler has been implemented in high-resolution frequency dividers. It is suitable for the wireless communication system below 4 GHz. The operation of this proposed prescaler and frequency divider have also been silicon verified. The high-speed frequency divider is a key block in frequency synthesis. The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input frequency. A dual-modulus prescaler usually consists of a divide-by-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units. The operation of the divide-by-2/3 unit at the highest input frequency makes it the bottleneck of the prescaler design. The key parameters of high-speed digital circuits are the propagation delay and power consumption. The greatest working frequency of a digital circuit is computed and is given by

$$f_{\max} = 1/t_{pLH} + t_{pHL} \quad (1)$$

Where t_{pLH} and t_{pHL} are the propagation delay of gates, respectively. The total power consumption of the CMOS digital circuits is determined by the combination of switching and short circuit power. The switching power is straightly relative to the operating frequency and is given by the total of switching power at each one node as in

$$P_{\text{switching}} = \sum f_{\text{clk}} C_{LiV}^2 V_{dd} \quad (2)$$

Where n is the quantity of switching nodes, f_{clk} is the clock frequency, C_{LiV} the load capacitance at the yield hub of the i th stage, and V_{dd} is the supply voltage. Typically the short circuit power happens in dynamic circuits when there exists immediate ways from the supply to ground which is given by

$$P_{\text{sc}} = I_{\text{sc}} * V_{dd} \quad (3)$$

Where I_{sc} is the short circuit current. The investigation in ETSPC demonstrates that the short circuit power is much higher in E-TSPC circuits than in TSPC circuits. Then again, TSPC logic circuits display higher switching power contrasted with that of E-TSPC logic circuits because of high load capacitance. For the E-TSPC logic circuit, the short circuit power is the real issue.

The E-TSPC circuit has the value of higher operating frequency than that of the TSPC circuit because of the decrease in load capacitance, however it devours essentially more power than the TSPC circuit accomplishes for a given transistor size. The accompanying analysis is focused around the most recent configuration utilizing the prominent and minimal effort 0.18/1 CMOS process.

3. WIDEBAND E-TSPC 2/3 PRESCALER

A Prescaler is an electronic counting circuit used to reduce a high frequency electrical signal to a lower frequency by integer division. A dual modulus prescaler is an electronic circuit used in high-frequency synthesizer designs to overcome the problem of generating narrowly-spaced frequencies that are nevertheless too high to be passed directly through the feedback loop of the system. The modulus of a prescaler is its frequency divisor. A dual-modulus prescaler has two separate frequency divisors, usually M and $M+1$. The E-TSPC 2/3 pre-scaler consumes large short circuit power and has a higher frequency of operation than that of TSPC 2/3 prescaler. The wideband single-phase clock 2/3 prescaler in this design consisting of two D flip-flops and two NOR gates embedded in the flip flops. The E-TSPC divide-by-2 unit has the merit of high operating frequency compared with the traditional TSPC divide-by-2 unit. In a simplified topology of the divide-by-4/5 unit is designed to achieve high operating frequency. To make less components work at full speed, a divide-by-2/3 is used here. Since the divide-by-2/3 unit consists of two toggle DFFs and additional logic gates, one way to effectively reduce the delay and power consumption is to integrate the logic gates to the divide-by-2/3 unit. In a gate-integrated dual-modulus prescaler based on the dynamic circuit has been proposed to achieve the high

operating frequency and low power consumption. This design uses two DFFs, while the divide-by-4/5 unit uses three DFFs.

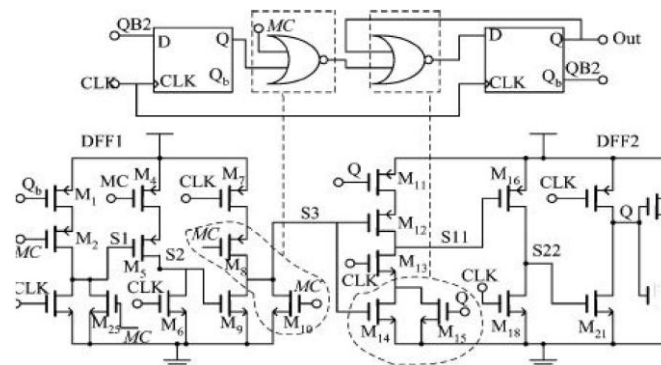


Fig.2. Wideband Single phase Clock 2/3 Pre-scalar

When the modulus control signal MC is logically low, it performs the divide-by-3 function. If the output of DFF2 is logically low, the node S1 of DFF2 is disabled, thus nodes S2 and S3 of DFF2 will have no switching activities, therefore, no switching power dissipation. DFF1 operates all the time, while DFF2 only operates when the output of DFF2 is logically high. When MC is logically high, the output of DFF1 will be disabled to achieve the divide-by-2 function. The first NOR gate is embedded in the last stage of DFF1, and the second NOR gate is embedded in the first stage of DFF2. Here, the transistors M2, M25, M4, M8 in DFF1 helps to eliminate the short-circuit power during the divide-by-2 operation. The switching of division ratios between 2 and 3 is controlled by logic signal MC. The load capacitance of the pre-scalar is given by

$$C_{L\text{-wideband}} = C_{dbM19} + 2C_{gdM19} + C_{dbM21} + 2C_{gdM21} + C_{Gm1} \quad (1)$$

When MC switches from "0" to "1," transistors M2, M4 and M8 in DFF 1 turns off and nodes S1, S2 and S3 switch to logic "0." Since node S3 is "0" and the other input to the NOR gate embedded in DFF2 is Qb, the wideband prescaler operates at the divide-by-2 mode. During this mode, nodes S1, S2 and S3 switch to logic "0" and remain at "0" for the entire divide-by-2 operation, thus removing the switching power contribution of DFF1. Since one of the transistors is always OFF in each stage of DFF1, the short-circuit power in DFF1 and the first stage of DFF2 is negligible.

The total power consumption of the pre-scalar in the divide-by-2 mode is equal to the switching power in DFF2 and the short-circuit power in second and third stages of DFF2 and is given by

$$P_{\text{wideband-divide-by-2}} = \sum_i f_{\text{clk}} C_{Li} V_{dd}^2 + P_{SC1} + P_{SC2} \quad (2)$$

Where C_{Li} is the load capacitance at the output node of the i th stage of DFF2, and P_{SC1} and P_{SC2} are the short circuit powers in the second and third stages of DFF2. When logic signal MC switches from "1" to "0," the logic value at the input of DFF1 is transferred to the input of DFF2 as one of the input of the NOR gate embedded in DFF1 is "0" and the wideband prescaler operates at the divide-by-3 mode. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1. Thus, the wideband 2/3 prescaler has benefit of saving more than 50% of power during the divide-by-2 operation. The measured result shows that the wideband 2/3 prescaler has the maximum operating frequency of 6.5GHz.

4. MULTIMODULUS 128/129/191/192 PRESCALER

The proposed wideband multi modulus prescaler which can divide the input frequency by 128, 129, 191 and 192. It is same as that of the 128/129 prescaler but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide-by-191 and divide-by-192) without any extra flip flop thus saving a considerable amount of power and also reducing the complexity of multiband divider.

In this frequency synthesizer, there is a block called multi-modulus divider. It is basically a block that divides the VCO output frequency by certain modulus decided by the delta-sigma modulator bits. It is a key part in realizing the fractional division, which is unique to fractional-N architecture. The multi-modulus divider system architecture is depicted in Fig 1. It consists of a chain of divide-by-2/3 dual-modulus prescalers in cascade, connected like a ripple counter.

The operation of multi-modulus, in every division period, the last cell of dual-modulus prescaler in the chain generates signal $\text{mod}n-1$. This signal then propagates up the chain. An active mod signal would enable the cell to divide by three once in a division cycle, as long as the programmable input bit p is set.

In other word, the dual-modulus divide-by-2/3 cell would divide by five only ONCE in a whole division cycle, if it ever gets enabled to do so by having both the programmability p and the signal mod enabled. For the rest of the division cycle, the cell divides the input by two. Thus, division-by-five action only adds one extra period

of each cell's input signal to the period of output signal. For example, each divide-by-five action in a cell with a 2.5 GHz (0.4ns period) input would introduce an extra 0.4 ns to the output period.

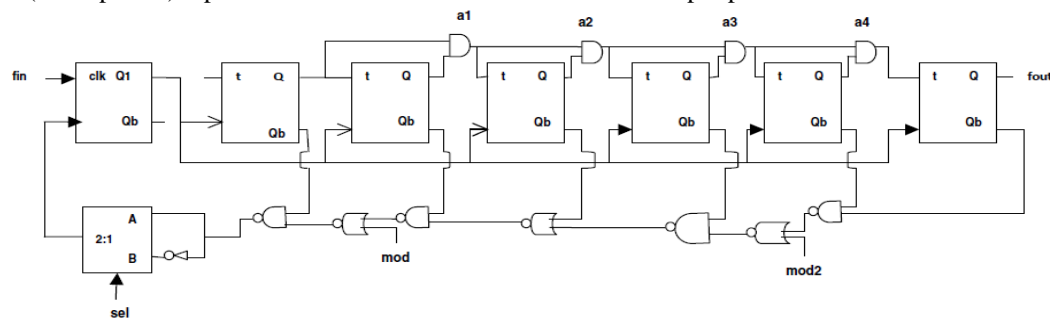


Fig.3. Propose multimodal's 128/129 and 191/192 prescaler

1) Case 1: sel='0'

When sel='0', the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multi modulus prescaler operates as the normal 128/129 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates in the divide-by-2 mode and when MC=0, the 2/3 prescaler operates in the divide-by-3 mode. If MOD=1, the NAND2 gate output switches to logic "1" (MC=1) and the wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multi modulus prescaler is

$$N = (AD*N1)+(0*(N1+1))=128 \quad (1)$$

Where N1=2 and AD=16 is fixed for the entire design. If MOD=0, for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the Divide-by-3 mode. The division ratio N+ 1 performed by the multi modulus prescaler is

$$N+1 = ((AD-1)*N1) \quad (2)$$

And S2 switch to logic "0" and the bit-cell does not perform any function. The MOD signal goes logically high only when the S-counter finishes counting down to zero. If MOD and LD are logically low, the bit-cell acts as a divide-by-2 unit. If MOD is logically low and LD is logically high, the input bit PI is transferred to the output. In the initial state, MOD=0, the multi modulus prescaler selects the divide-by-N+ 1 mode (divide-by-33)

2) Case 2: sel = '1'

When sel=' 1', the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multi modulus prescaler operate as a 191/192 prescaler, where the division ratio is controlled by the logic signal MOD. If MC= 1, the 2/3 prescaler operates indive-by-3 mode and when MC=0, the 2/3 prescaler operates indive-by-2 mode which is quite opposite to the operation performed when sel='0' If MOD=1, the division ratio N+ 1 performed by the multi modulus prescaler is same except that the wideband prescaler operates in the divide by-3 mode for the entire operation given by

$$N+1 = (AD*(N1+1))+(0*N1)=192 \quad (3)$$

If MOD=1, the division ratio N performed by the multi modulus prescaler is the logic implementation of the 2/3 divider cell requires D latches and AND gates.

$$N = ((AD-1)*(N1+1))+(1*N1)=191 \quad (4)$$

There are many designs for digital latches available, such as the built-in libraries offered by many standard CMOS process. But the multi-modulus divider chain in the frequency synthesizer serves to reduce the output frequency of the VCO to the reference frequency. Thus the input clock frequency for the first dual-modulus cell could be as high as 1.6 GHz to 2.5 GHz. Off the shelf digital blocks does not necessarily work under such high frequency. An appropriate circuit topology should be chosen to meet the high speed requirement. Complementary Metal Oxide Semiconductor (CMOS).

5. MULTIBAND FLEXIBLE DIVIDER

The single-phase clock multiband flexible divider consists of the multi modulus 128/129/191/192 prescaler, a 7-bit programmable P-counter and a 6 bit swallow S-counter. The control signal Sel decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5-5.825 GHz). Most of the CMOS frequency synthesizers reported in the literature use CML logic dividers as first stage dividers. The multi-band fully programmable divider for the 2.4 GHz ISM band and the 5 GHz WLAN band with a flexible resolution. The multi-band divider consists of the proposed multi-modulus 128/129/191/192 prescaler, a 7-bit programmable P-counter and a 6-bit swallow S-counter. The implementation of channel selection in a PLL frequency synthesizer requires programmable frequency dividers operating at high frequency. The most straightforward way to implement a divide-by-2 digital frequency divider is to use a toggle flip-flop., a T-FF can be implemented.

Swallow (S) Counter

The Swallow Counter is one of the three building blocks (swallow counter, main counter, and dual-modulus prescaler) that constitute the programmable divider commonly used in modern frequency synthesizers using a D-FF feeding back the negate output /Q to the input D. The input clock to be divided is then provided at the CLK input.

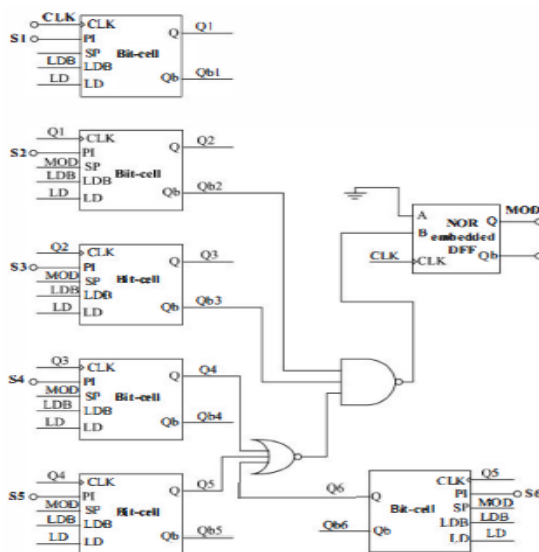


Fig 4 Asynchronous 6 bit S Counter

The swallow counter is used to control the dual-modulus prescaler which is set to either N or $(N+1)$. At the initial reset state, the prescaler is set to a divide ratio of $(N+1)$, but the swallow counter will change this divide ratio to N when it finishes counting S number of cycles.

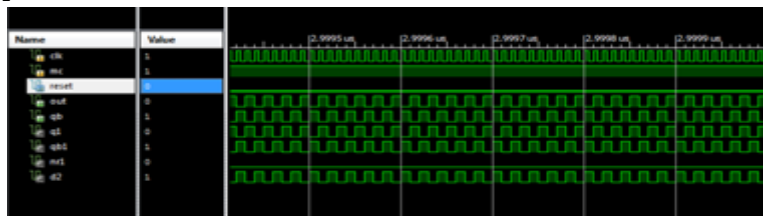
A pulse-swallowing counter is a component in an all-digital feedback system. The overall pulse-swallowing system is used as part of a fractional- N frequency divider. The 6-bit s-counter shown in Fig.4 consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high frequency band.

Programmable (P) Counter

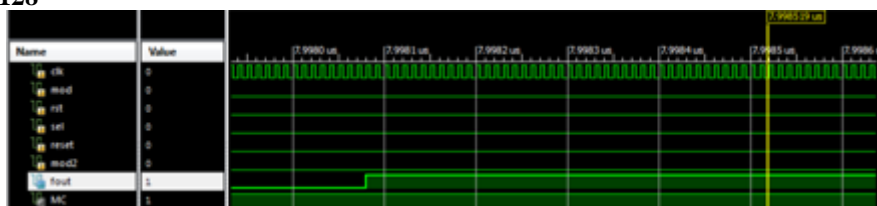
Programmable timer or counter is used for generation of an accurate time delay, for event counting rate generation, complex waveform generation applications, and so on. The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P7 is tied to the Sel signal of the multi modulus prescaler and bits P4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" ($MOD=0$) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. Thus, the multimodulus 128/129/191/192 prescaler eases the design complexity of the P-counter.

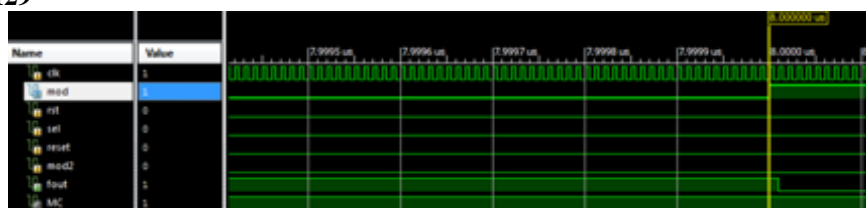
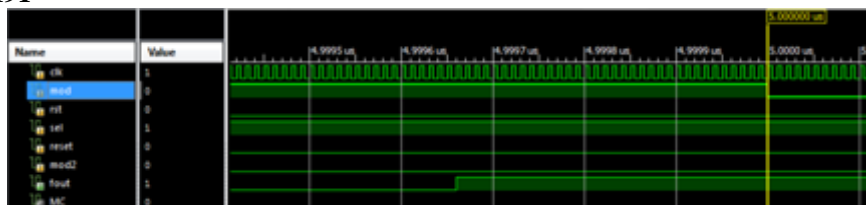
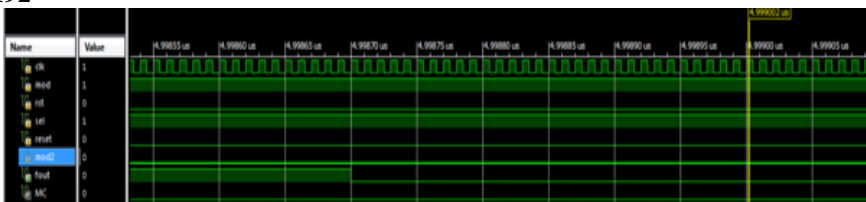
6. SIMULATION RESULTS

E-tspc 2/3 prescaler



DIVIDE-BY-128



DIVIDE-BY-129**DIVIDE-BY-191****DIVIDE-BY-192****7. CONCLUSION**

Here we are designing the 128/129/191/192 prescaler by using 2/3 prescaler. In this paper a simple approach for the low power single phase clock distribution for Wireless Local Area Networks frequency synthesizer is presented. The technique for low power fully programmable divider using design of reload able bit cells for P and S Counter is given. P and S counters can be programmed accordingly for the required bands of frequencies. Here the clock divider uses a wide band 2/3 prescaler and a multi modulus prescaler. By using this multi modulus prescaler, the Clock Jitter can be avoided.

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