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DESIGN OF LOW POWER SEQUENTIAL CIRCUITS BY USING CLOCKED PASS TRANSISTOR FLIP FLOP

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ABSTRACT

Clocks distribution networks (CDN's) play a vital role in synchronous circuits. The clock distribution network distributes the clock signal to the all sequential elements in the synchronous system. There is several designs are proposed to design efficient clock distribution networks. Very much concentration has been given to the characteristics of the clock signals and electrical networks used in their distribution. This paper discusses the clocked pass transistor flip flop to design the low power sequential circuits.

Keywords: *CDN, Flip-Flops, Low Power*

1. INTRODUCTION

Clock signals are plays a significant role in synchronous circuits. Different data signals are synchronized by the clock signals which are coming from the different parts of the IC (Integrated circuit), such that the computation can be done with correct data. The interconnects are presented with impedances. Due to these impedances there are mismatches in the clock coming time caused by spatial distances between two clocks. These are known as clock skews due to mismatches in time. Interconnect lines are running parallel with clock signals which are effect by noises so that the clock signals arrives at different registers with the same clock input which experience a phase noise. These are simply known as clock Jitter.

In synchronous system Clock Network play an important role in influence the speed, area, and power dissipation of the system. CDNs make sure that these constraints regarding clock skew and jitters are minimized. However the design of clock distribution networks are difficult task and designer must decide the clock distribution before the circuit is designed because difficulty increases in efficient CDN in latter stages. Various CDN's structure have been developed given that the routing area and complexity, speed, and power dissipation of the system are all factors changes by the clock network design.

Diverse strategies are utilized to fulfil the clock conditions given above. Such methods include a tree like structure that has a fundamental "trunk" supplying the global clock which branches at different points in the circuit focused around the loads. Such clock distribution networks incorporate cushioned clock distribution network, H-tree, X-tree distribution network, and mesh type CDN. To guarantee that clock load is adjusted at each branch of the clock tree in a H-tree or X-tree network, interconnect that conveys these clock sign are scaled by 1/3 at each branch.

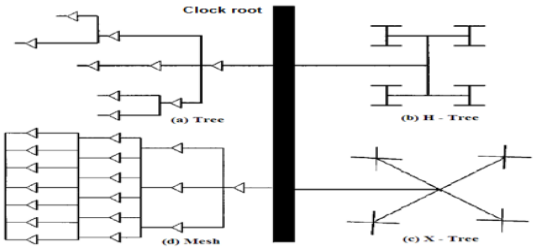

Fig 1: Clock Distribution Network Structure

2. CDN TYPES

2.1 Square wave CDN:

Square Wave CDN consists of Buffers, which are used to drive different sections in the tree

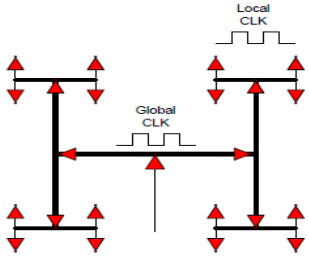

Fig 2: Square Wave CDN

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2.2 Globally-resonant locally-square CDN:

An inductor is connected at the centre of the H-tree in order to generate a resonating clock signal at the original frequency of the clock node. Lower branches of the H-tree are driven by buffers which in turn convert the sinusoidal clock to square-wave signal feeding the flip-flops

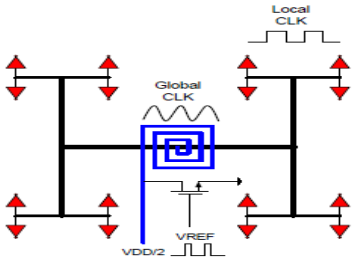

Fig 3 :Globally resonant locally square CDN

2.3 Fully resonant CDN:

LC resonant CDNs in addition to their low-power consumption have the advantage of generating a clock signal with uniform phase and amplitude. It also requires minimum change from conventional square-wave design.

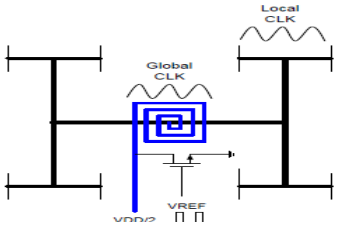

Fig 4: Fully resonant CDN

3. SOLUTION

Clock system consists of Clock generator, CDN and Flip-flops/latches in-order reduce the driving load of CDN conventional buffers are replaced with the fully LC resonant circuits, so that we can reduce the power dissipation caused by the CDN. LC resonant CDNs in addition to their low-power consumption have the advantage of generating a clock signal with uniform phase and amplitude. It also requires minimum change from conventional square-wave design. In-order to reduce Flip-Flops power dissipation we introduced different flip-flops like Pulse triggered Flip-Flops reduced size of flip flop to single latch and to reduces the redundancy discharge problems in TSPC latch many Conditional based techniques are introduced like conditional Capture, Conditional Discharge and Conditional Data Mapping techniques are proposed. Above techniques reduced the unwanted discharging of TSPC latch when static input "1" case but drawback of the system was number of clocked transistors which influences in more dynamic power dissipation. So in-order to reduce the dynamic power dissipation we proposed a Clock Pair Shared Flip-Flop which has 4 Clocked Transistors.

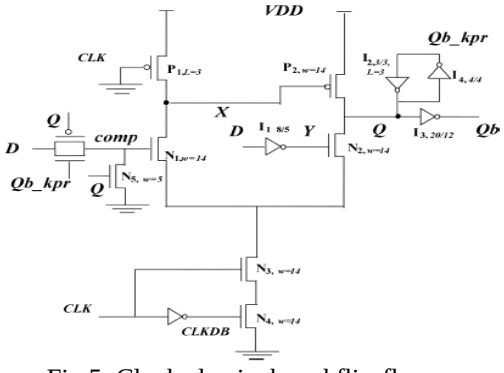

Fig 5: Clocked pair shared flip-flop

Clocked Pair Shared flip-flop (CPSFF)[6]is use less clocked transistor. In the clocked-pair-shared flip-flop, clocked pair is shared by first and second stage. An always ON PMOS, P1, is used to charge the internal node charging here we consider PMOS in pseudo PMOS structure. The data gating was done whenever the input was at static 1 case, the data was gated by using the input transmission whose inputs are Q and Qbar. Whenever data transmits from low to high then data was allowed by transmission gate, once output was generated it stops the data, so when data transmits from1-1 it will have no discharging of internal node. In CPSFF we reduces the number of clocked transistors as well as unwanted discharging of flip-flops.

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LC resonant clocking requirements the smallest amount change from conventional CDN design caused by the constant phase and amplitude of the clocked signal.LC resonant clocking up to this date, is the most developed and useful resonant clocking technique. The clocking scheme adopted and assumed in this dissertation from here on is the fully-resonant LC scheme. The clock signal feeding the flip-flops is assumed to be purely sinusoidal clock since extending the resonance down to the flip-flop level results in most power savings as discussed previously.

Any flip-flop can operate at both square and/or sinusoidal clocks since a sine-wave can be considered as a square-wave with longer rise and fall times. In the following, a brief description of two flip-flops that were proposed in the literature as energy-recovery flip-flops that operate with a sinusoidal clock will be presented

3.1 Low Swing Differential Conditional Capturing Flip-Flop (LS-DCCFF):

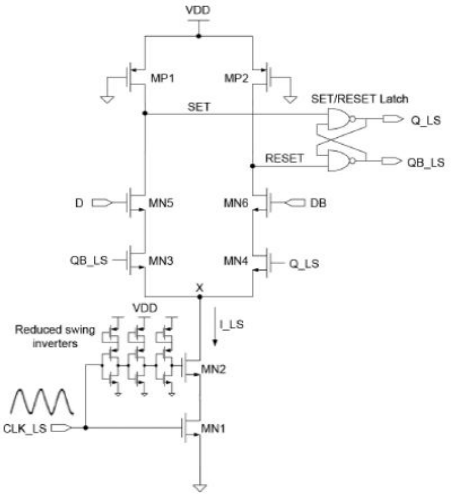

Fig 6: LS-DCCF flip flop

The LS-DCCFF is shown in Figure 6. In order to minimize flip-flop power dissipation at low data switching actions by eliminating redundant internal transitions conditional capturing is used. Reduced swing inverters are fed by low swing sinusoidal clock signal. This is used to avoid the short circuit power. In the reduced swing inverters the load PMOS transistor is in always saturation since Vgs=Vds. Due to this the voltage at the source of the second PMOS transistor reduces in each inverter to approximately Vdd-|Vtp| thus it turns off when the low swing sinusoidal clock signal reaches its peak voltage.

When both MN1 and MN2 are in ON state , D=0 and Q_LS=0 then the QB_LS=1 then the SET node and RESET nodes connected to Vdd. This case the output becomes in low state . When D=1 and QB_LS=1 then the SET node connected to ground so the output becomes high. This technique reduces the power dissipation compared to previous technique.

3.2 Clocked pass transistor Flip flop:

By using the Pass Transistor Logic family idea we are designing this circuit as well as by using the pass transistor logic we are using only one clocking transistor so it will be consuming only less power in the clock network of the Flip flop when compared to all further circuits. Here only 6 Transistors without the NOT gates also. So that the power and area were reduced much compared to previous designs. In this design the transistor count reduces significantly due to this delay always reduces. Thus we are reducing the power consumption, area and overall switching delays. So this circuit will be acting as good sequential elements when compared to other flip-flop design.

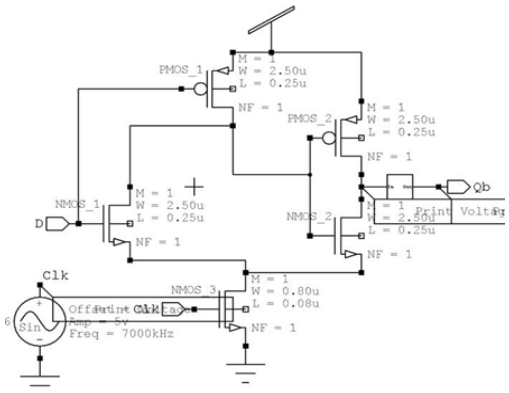

Fig 7: Clocked pass transistor flip flop

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4. SIMULATION AND RESULTS

These circuits are designed and simulated using the Tanner Tools with TSMC 018 Technology. The simulation results for LS-DCCF is shown below.

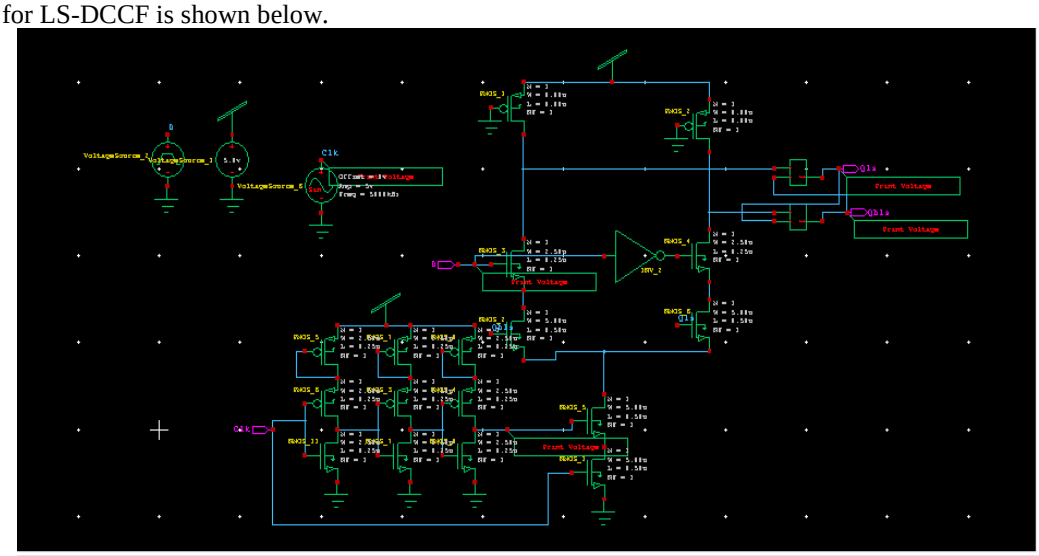

Fig 8: LS-DCCF Flip flop schematic representation

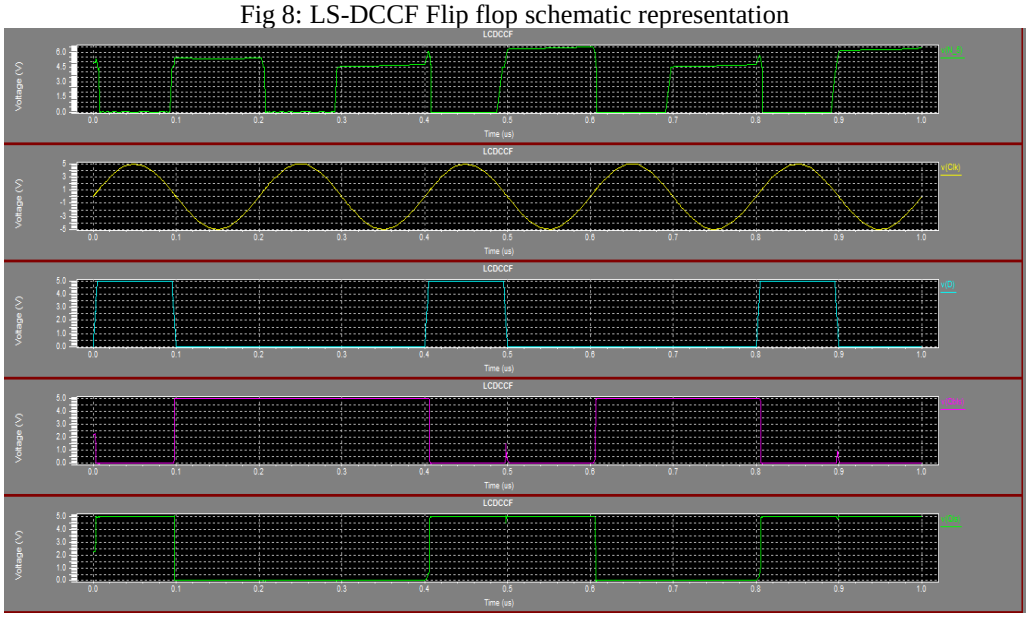

Fig 9: Simulated waveforms for LSDCCF

The simulation results for the clocked pass transistor flip flop in the form of wave forms are shown in below figures.

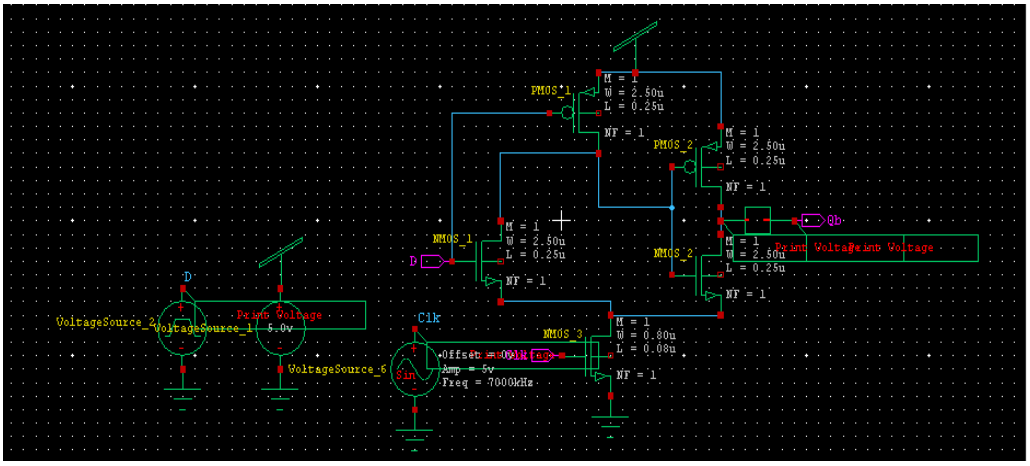

Fig 10: Schematic representation for clocked pass transistor flip flop

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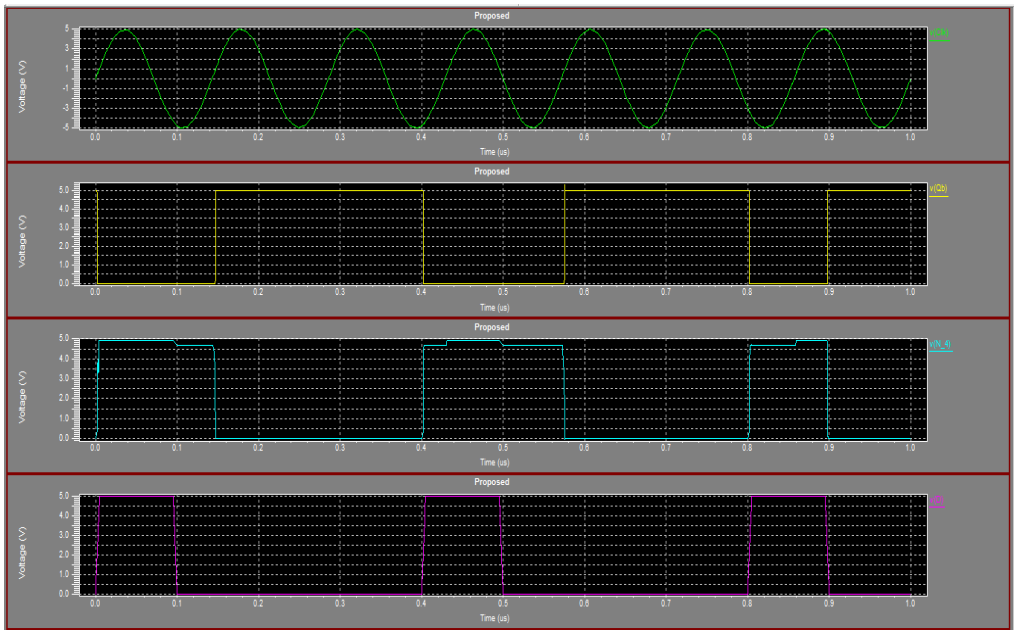

Fig 11: Simulated waveforms for clocked pass transistor flip flop

The simulations results for the above circuits in the form of power dissipation are shown in the below table.

Circuit	Power dissipation
CPFF	4.665e-004watts
LS-DCCF	1.725e-004watts
Clocked pass transistor flip flop	3.32e-006watts

5. CONCLUSION

In this Paper we analyses the various Clock distribution networks, fully LC resonant Clock Distribution Network which has less power consumption in CDN networks. The proposed Clocked Pass Transistor flip-flop produces a less power consumption than existing ones. It show high performance for future applications.

REFERENCES

[1] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 807–811, May 1998.
[2] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high speed sense-amplifier-based flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 11, pp. 1266–1274, Nov. 2005.
[3] H. Partovi, R. Burd, U. Salim, F.Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *IEEE Tech. Dig. ISSCC*, 1996, pp. 138–139.
[4] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R.Wang, A. Mehta, R. Heald, and G.Yee, "A newfamily of semi-dynamic and dynamic flip flops with embedded logic for high-performance processors," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 712–716, May 1999.
[5] S. D. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. J. Sullivan, and T. Grutkowski, "The implementation of the Itanium 2 microprocessor," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1448–1460, Nov. 2002.
[6] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in *Proc. ISPLED*, 2001, pp. 207–212.
[7] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.
[8] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power-efficient dual-edge clocking," in *Proc. Int. Symp. Low-Power Electron. Design*, Monterey, CA, Aug. 12–14, 2002, pp. 56–59.
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