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BUILT-IN GENERATION OF FUNCTIONAL BROADSIDE USING FIXED HARDWARE STRUCTURE

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ABSTRACT

In this proposed method we are test 36-bit input ISCAS-85 C432 27-channel interrupt controller. This paper described an on-chip test generation method for functional broadside tests. The hardware was based on the application of primary input sequences starting from a known reachable state, thus using the circuit to produce additional reachable states. Random primary input sequences were modified to avoid repeated synchronization and thus yield varied sets of reachable states. Two-pattern tests were obtained by using pairs of consecutive time units of the primary input sequences. The hardware structure was simple and fixed, and it was tailored to a given circuit only through the following parameters: the length of the LFSR used for producing a random primary input sequence; the length of the primary input sequence; the specific gates used for modifying the random primary input sequence; the specific gate used for selecting applied tests; and the seeds for the LFSR. With the proposed on-chip test generation method, the circuit is used for generating reachable states during test application. This alleviates the need to compute reachable states offline.

I. INTRODUCTION

Over testing due to the application of two-patterns can-based tests was described in [1]–[3]. Over testing is related to the detection of delay faults under non-functional operation conditions. One of the reasons for these non-functional operation conditions is the following. When an arbitrary state is used as a scan-in state, a two-pattern test can take the circuit through state-transitions that cannot occur during functional operation. As a result, slow paths that cannot be sensitized during functional operation may cause the circuit to fail [1]. In addition, current demands that are higher than those possible during functional operation may cause voltage drops that will slow the circuit and cause it to fail [2], [3]. In both cases, the circuit will operate correctly during functional operation. Functional broadside tests [4] ensure that the scan-in state is a state that the circuit can enter during functional operation, or a reachable state. As broadside tests [5], they operate the circuit in functional mode for two clock cycles after an initial state is scanned in. This results in the application of a two-pattern test.

Since the scan-in state is a reachable state, the two-pattern test takes the circuit through state-transitions that are guaranteed to be possible during functional operation. Delay faults that are detected by the test can also affect functional operation, and the current demands do not exceed those possible during functional operation. This alleviates the type of over testing described in [1]–[3]. In addition, the power dissipation during fast functional clock cycles of functional broadside tests does not exceed that possible during functional operation.

Test generation procedures for functional and pseudo-functional scan-based tests were described in [4] and [6]–[13]. The procedures generate test sets offline for application from an external tester. Functional scan-based tests use only reachable states as scan-in states. Pseudo-functional scan-based tests use functional constraints to avoid unreachable states that are captured by the constraints.

This work considers the on-chip (or built-in) generation of functional broadside tests. On-chip test generation reduces the test data volume and facilitates at-speed test application. On-chip test generation methods for delay faults, such as the ones described in [14] and [15], do not impose any constraints on the states used as scan-in states. Experimental results indicate that an arbitrary state used as a scan-in state is unlikely to be a reachable state [4]. The on-chip test generation method from [16] applies pseudo-functional scan-based tests. Such tests are not sufficient for avoiding unreachable states as scan-in states. The on-chip test generation process described in this work guarantees that only reachable states will be used.

It should be noted that the delay fault coverage achievable using functional broadside tests is, in general, lower than that achievable using arbitrary broadside tests as in [14], [15] or pseudo-functional broadside tests as in [16]. This is due to the fact that functional broadside tests avoid unreachable scan-instates, which are allowed by the methods described in [14]–[16]. However, the tests that are needed for achieving this higher fault coverage are also ones that can cause over testing. They can also dissipate more power than possible during functional operation.

Only functional broadside tests are considered in this work. Under the proposed on-chip test generation method, the circuit is used for generating reachable states during test application. This alleviates the need to compute reachable states or functional constraints by an offline process as in [4], [6]–[13] and [16]. The underlying observation is related to one of the methods used in [4] for offline test generation, and is the following.

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If a primary input sequence A is applied in functional mode starting from a reachable state, all the states traversed under A are reachable states. Any one of these states can be used as the initial state for the application of a functional broadside test. By generating A on-chip and ensuring that it takes the circuit through a varied set of reachable states, the on-chip test generation process is able to achieve high transition fault coverage using functional broadside tests based on A. It should be noted that, for the detection of a set of faults F, at most |F| different reachable states are required. This number is typically only a small fraction of the number of all the reachable states of the circuit. Thus, the primary input sequence A does not need to take the circuit through all its reachable states, but only through a sufficiently large number relative to |F|, in order to be effective for the detection of target faults.

The hardware used in this paper for generating the primary input sequence A consists of a linear-feedback shift-register (LFSR) as a random source [17], and of a small number of gates (atmost six gates are needed for every one of the benchmark circuits considered). The gates are used for modifying the random sequence in order to avoid cases where the sequence takes the circuit into the same or similar reachable states repeatedly. This is referred to as repeated synchronization [18]. In addition, the on-chip test generation hardware consists of a single gate that is used for determining which tests based on will be applied to the circuit. The result is a simple and fixed hardware structure, which is tailored to a given circuit only through the following parameters.

1) The number of LFSR bits.
2) The length of the primary input sequence.
3) The specific gates used for modifying the LFSR sequence into the sequence.
4) The specific gate used for selecting the functional broadside tests that will be applied to the circuit based on.
5) Seeds for the LFSR in order to generate several primary input sequences and several subsets of tests.

The on-chip test generation hardware is based on the one described in [19]. It differs from it in the following ways.

2. FUNCTIONAL BROAD SIDE TESTING

2. 1 BLOCK DIAGRAM OF BROADSIDE AND FUNCTIONAL BROADSIDE TESTING

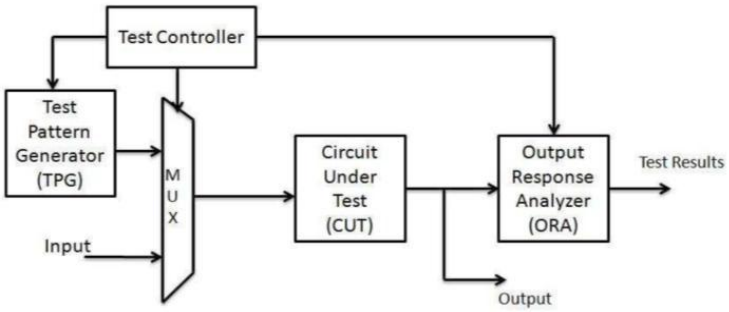

Fig: Simple BIST circuitry

2.2 BROADSIDE TESTS IN PARTIAL-SCAN CIRCUITS

In a full-scan circuit, a broadside test starts by scanning in a state denoted by two primary input vectors, denoted by and are then applied in functional mode. The final state reached at the end of the test is scanned out. The test can be partitioned into two patterns, applied in one functional clock cycle, and applied in a second functional clock cycle. The application of is done under a slow clock to allow signal transitions in the circuit to settle. The application of is done under a fast clock in order to capture delayed signal-transitions. Faults are detected by observing the primary output vector obtained in response to and when the final state is scanned out. In a full scan circuit, the scan-in state is a fully-specified state. After scanning in all the state variables of the circuit are assigned known values. In addition, the values of all the state variables are observed during the scan-out operation at the end of the test. For illustration, we consider a circuit with two primary inputs and five state variables, which are denoted by suppose that and are scanned, an that and are un scanned. A possible scan-in state is 000xx, where x stands for an unspecified (unknown) value. In a broadside test for this circuit, may be a partially-specified state as well. For example, suppose that with and we obtain 1x01x. Let we obtain the two-pattern test000xx 00, 1x01x 11. With partially- specified patterns, it may not be possible to activate certain faults. In addition, faults whose effects are propagated by the second pattern to or will not be detected by the scan-out operation at the end of the test. Therefore, it is necessary to consider broadside tests with more than two primary input vectors. The primary input vectors are then applied in functional mode. The state at time unit of the test, where is the next-state obtained when the present-state is and the primary input vector is There is one time unit where such that is applied under a fast clock in order to capture delayed signal-transitions. Application of for such that is done under a slow clock to allow signal-transitions in the circuit to settle. Under the slow clock the circuit operates as a fault free circuit.

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2.3 PESUDORANDOM TEST GENERATION

The three primary goals were:

(a) to develop a battery of statistical tests to detect non randomness in binary sequences constructed using random number generators and pseudorandom number generators utilized in cryptographic applications,

(b) to produce documentation and a software implementation of these tests, and

(c) to provide guidance in the use and application of these tests. Pseudorandom- generate patterns that appear to be random but are in fact deterministic (repeatable).Linear Feedback Shift Register (LFSR)

Weighted pseudo-random test generation Adaptive pseudo-random test generation

2.3.1 Algorithmic Test Generation

List primary inputs controlling location where a fault should be detected.

Determine primary input conditions to activate a fault and to sensitize the primary outputs such that the fault can be observed.

2.3.2 Linear Feedback Shift Registers (LFSRs)

Efficient design for Test Pattern Generators & Output Response Analyzers (also used in CRC) FFs plus a few XOR gates better than counter

- Fewer gates
- Higher clock frequency
- Two types of LFSRs External Feedback, Internal Feedback
- Higher clock frequency

An LFSR generates periodic sequence must start in a non-zero state, The maximum length of an LFSR sequence is 2n -1 does not generate all 0s pattern (gets stuck in that state)The characteristic polynomial of an LFSR generating maximum-length sequence is a primitive polynomial A maximum-length sequence is pseudo-random: number of 1s =number of 0s + 1 same number of runs of consecutive 0s and 1s 1/2 of the runs have length1 1/4 of the runs have length 2 (as long as fractions result in integral numbers of runs).

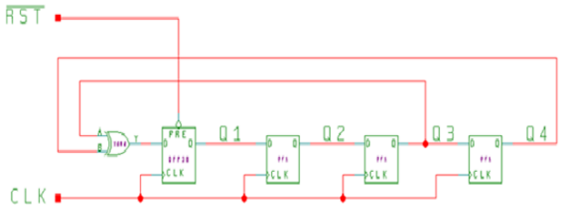

Figure : LFSR 4bit circuit

2.4 COMBINATIONAL BENCHMARK CIRCUIT C432

Several Industry standard benchmark circuits such as ISCAS-85, ISCAS-89, etc can be used to test new design, test and manufacturing approaches and technologies. Following is a brief description of one of the ISCAS-85 circuits used for the purpose of testing the new low power pattern generation scheme described above.

C432 is a 27-channel interrupt controller. The input channels are grouped into three 9-bit buses (we call them A, B and C), where the bit position within each bus determines the interrupt request priority. A forth 9-bit input bus (called E) enables and disables interrupt requests within the respective bit positions. Figure below shows the c432 circuit. Figures below show the logic of the underlying modules.

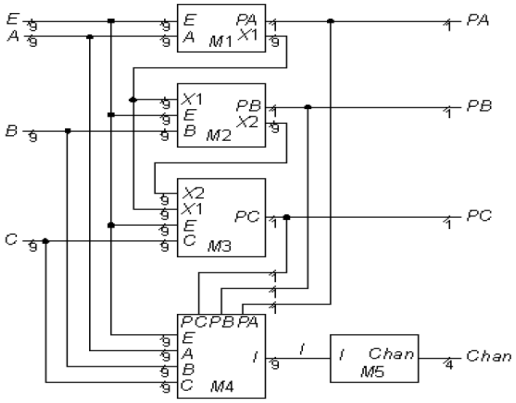

Figure : C432 Combinational Circuit

- Logic Gates are taken at Primary input combination in (2^36).

Statistics: 36 inputs; 7 outputs; 160 gates; bus translations

Function: c432 is a 27-channel interrupt controller. The input channels are grouped into three 9-bit buses (we call them A, B and C), where the bit position within each bus determines the interrupt request priority. A forth 9-bit input bus (called E) enables and disables interrupt requests within the respective bit positions. The figure

Vol 05, Article 09416, September 2014
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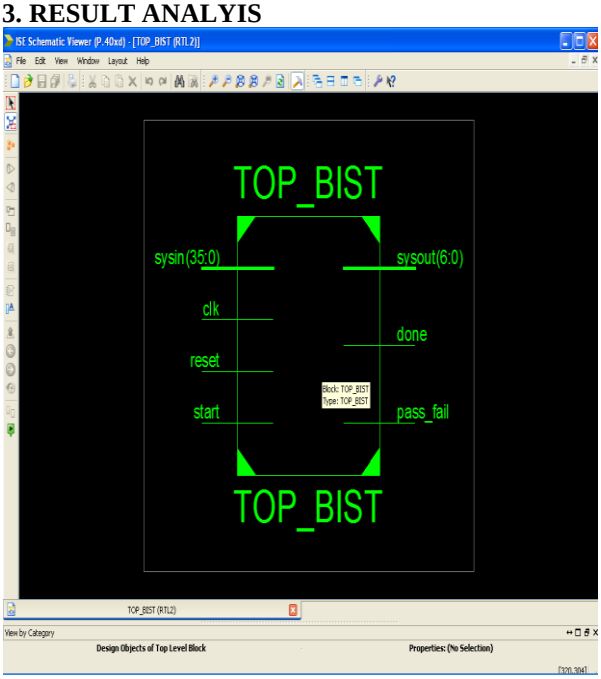
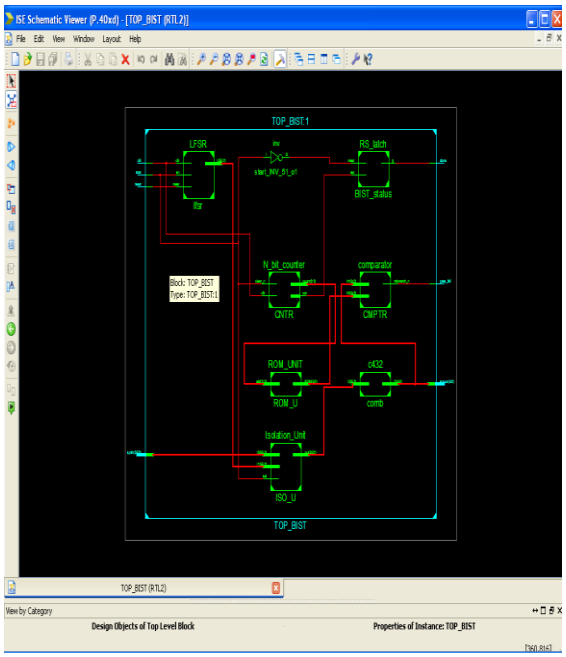
above concisely represents the circuit. The figure above contains the modules labeled M1, M2, M3, M4, and M5, which contain the underlying logic.

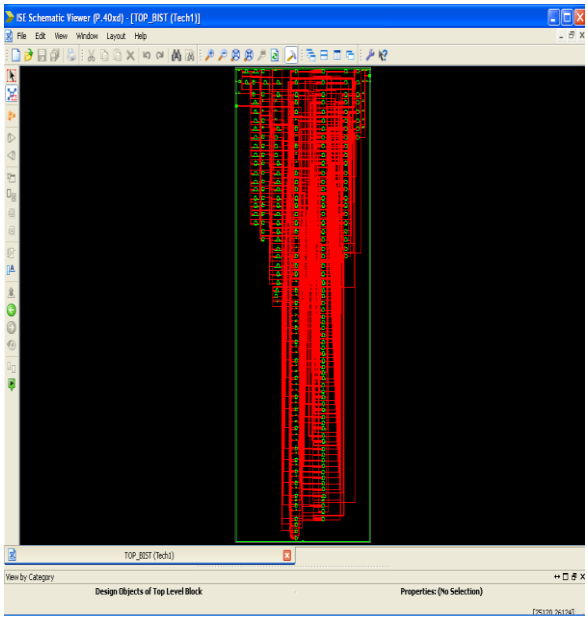
3. RESULT ANALYIS



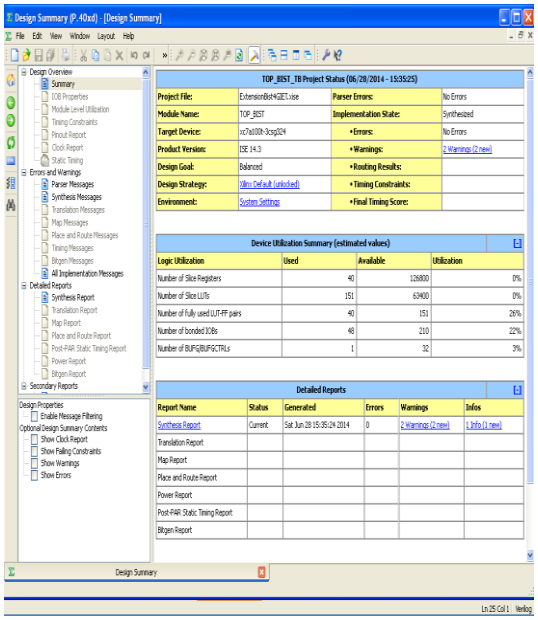
BLOCK DIAGRAM



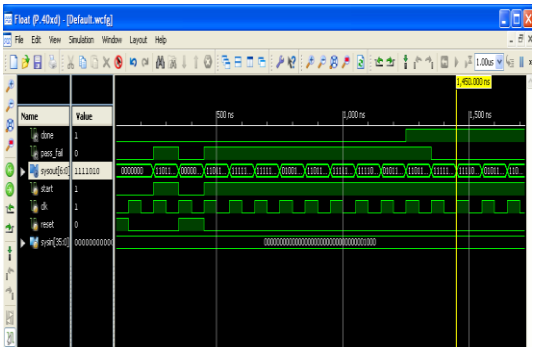
RTL SCHEMATIC



TECHNOLOGY SCHEMATIC DIAGRAM



DESIGN SUMMARY



OUTPUT WAVEFORM

Vol 05, Article 09416, September 2014 International Journal of VLSI and Embedded Systems-IJVES
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CONCLUSION

The presence of delay-inducing defects is causing increasing concern in the semiconductor industry today. To test for such delay-inducing defects, scan-based transition fault testing techniques are being implemented. To Full scanning Process will Generated and then Fault coverage for Broadside testing is 80% , functional broadside testing is 40% and Pseudorandom testing is 80%. Maximum length of the testing is 362. Full scanning percentage is 97.5%. Fault coverage for the Broadside testing with s_t_0 Fault will generate in above circuit is 85%. Maximum length of testing full scan circuit is 402. Scanning percentage is 97%. Testing time for partial scan process is reduces Maximum testing length is reduced at 284. Fault coverage is maximum one of partial scan process.

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