

# High Frequency Power Optimized Ring Voltage Controlled Oscillator for 65nm CMOS Technology

NEHA K.MENDHE<sup>1</sup>, M. N. THAKARE<sup>2</sup>, G. D. KORDE<sup>3</sup>

Department of EXTC, B.D.C.O.E, Sevagram, India,

[nehakmendhe02@gmail.com](mailto:nehakmendhe02@gmail.com)<sup>1</sup>, [mnt\\_ent@rediffmail.com](mailto:mnt_ent@rediffmail.com)<sup>2</sup>, [gdkorde@gmail.com](mailto:gdkorde@gmail.com)<sup>3</sup>

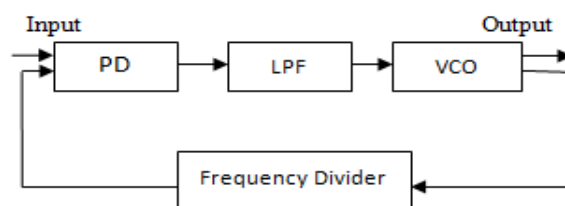
## ABSTRACT

Voltage Controlled Oscillator (VCO) is key building block of Phase Locked Loop (PLL) and Radio Frequency (RF) communication system. The design of high performance VCOs has been increasingly more important and still is an active research area. Research on VCOs for the past decade has been concentrated in the areas of higher frequency, lower phase noise, low power, low operating voltage, and increased tuning range. Among the architectures of VCO, Ring Oscillator shows better performance so it is selected for the research. The VCO exhibit at high frequency tuning range from 1.06-1.17GHz; its power consumption is only 8.63mW. The circuit is simulated in Tanner Tool version-13 environment. The optimization design and layout are done using S-EDIT software to make the oscillator as small as possible. In addition, T-spice and W-EDIT tools are used in the analysis and simulation to verify the predicted performance.

**Index Terms-** CMOS, Phase noise, ring oscillator, voltage controlled oscillator (VCO).

## 1. INTRODUCTION

Phase Locked Loops (PLL) is an essential for the synchronization purposes in space communication. PLLs are also widely employed in radio, telecommunications, computers and others electronic applications. PLL is composed of phase detector (PD), low pass filter (LPF), voltage controlled oscillator (VCO) and frequency divider. Voltage Controlled Oscillator (VCO) is vital part of PLL; its performance has strong impact on the PLL



**Fig-1:** Block diagram of PLL

The VCO frequency is tuned such that it will shift to the reference frequency until the error signal comes down to zero. VCO generates frequency and changes the oscillating frequency varying control voltage. Hence the low power consumption VCO improves the performance of the PLL. An oscillator that changes its frequency according to a control voltage feed to its control input is Voltage Controlled Oscillator.

CMOS VCO can be designed using two types of structures, LC oscillators and Ring oscillators. LC oscillator is design by using inductor and capacitor. LC based VCO has narrow tuning range, greater power dissipation and large die area. In addition, it is very difficult to integrate inductor in digital CMOS technology. Ring oscillator is composed of delay stages along with the feedback from output to input stage. Ring oscillator provides wide tuning range, relatively constant voltage swing and low voltage operation. Ring VCO requires less chip area and can be built in any standard CMOS processes.

VCRO can be implemented by single-ended or differential architecture of delay cell. Single ended ring topology comprises of inverters and each inverter is made up of an NMOS and PMOS transistors. On the other hand, differential topology is made up of a load (active or passive) with a NMOS differential pair. Currently, differential circuit topology is getting popularity among designers as it has common mode rejection of supply and substrate noise. In this paper, the low power consumption single delay cell for Ring VCO is implemented in 65nm CMOS technology.

In this paper, a CMOS four-stage differential ring oscillator is analyzed using 65 nm technology proposed by Joo-Myoung Kim [1]. It is redesigned by varying the design parameters to achieve high tuning range and low power consumption. Comparison with other oscillators is made to illustrate the advantages of this design.

The paper is organized as follows: Section 2 discusses the details of oscillator design, section 3 describes delay cell architecture simulation results and a conclusion is drawn in Section IV.

## II. CIRCUIT DESIGN

### VCRO ARCHITECTURE

Fig 2 shows the circuit design of proposed four stage ring VCO.

The feedback circuit's transfer function for oscillator is given by equation (1).



$$\frac{V_{out}}{V_{in}} = \frac{H(S)}{1 + H(S)} \quad (1)$$

Where, H(s) is feedback function of oscillator.

The Barkhausen criteria for oscillation which govern condition for oscillators are given by,

$$|H(s)| \geq 1 \quad (2)$$

$$\angle H(s) = 180^\circ \quad (3)$$

These conditions are necessary but may not be sufficient to ensure oscillation. A VCO is an oscillator whose open loop transfer function H(s) can be varied by a control voltage. Fig. 2 shows the four stage Ring VCO architecture. The oscillator satisfied the Barkhausen criterion. The open loop transfer function for the ring VCO is given by equation

$$H(S) = -\frac{A_{04}}{\left(1 + \frac{S}{W_0}\right)^4} \quad (4)$$

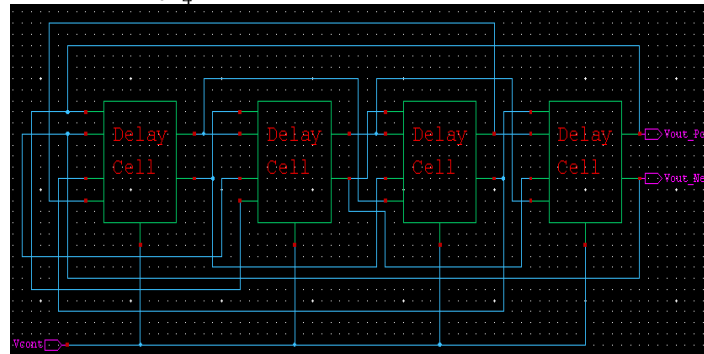


Fig. 2: Four Stage Ring VCO

In this work the concentration is provide to reduce the power consumption by adjusting the supply voltage and input frequency. The oscillation frequency of a ring VCO with  $N$  stages of identical delay cells is express in equation (2).

The oscillation frequency is inversely proportional to the number of delay stages.

$$F_{ring} = \frac{1}{N \cdot t_{delay}} \quad (5)$$

Where  $N$  is the number of stages and  $t_{delay}$  is the delay time for each stage. For every signal cycle, there is a downward as well as an upward transition. Since the high-to-low ( $t_{pHL}$ ) and low-to-high ( $t_{pLH}$ ) propagation delays associated with these transitions are not usually equal, the average propagation delay is given by

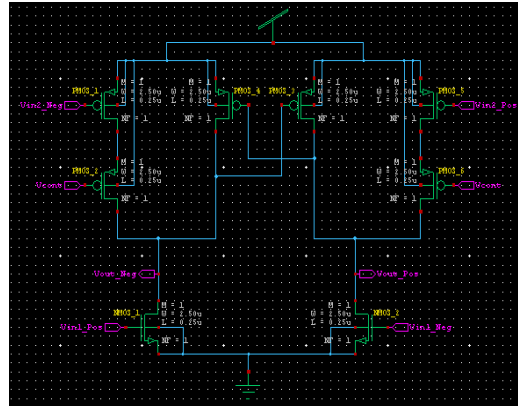
$$T = \frac{(t_{pHL} + t_{pLH})}{2} \quad (6)$$

In VCO Phase noise is the frequency domain representation of rapid, short-term, random fluctuations in the phase of a waveform, caused by time domain instabilities. An oscillator can be considered as a filtered noise generator and therefore noise will surround the carrier. The phase noise describes the fluctuation of the oscillation frequency. In the proposed VCRO by proper sizing the transistor lower down the phase noise. Due to which it is better than compared VCO model.

### III. DELAY CELL ARCHITECTURE

In this research, novel delay cell architecture for the VCRO has been proposed as shown in Fig. 4. The delay cell consists of the NMOS input transistors NMOS\_1 and NMOS\_2, the cross-coupled PMOS transistors PMOS\_4 and PMOS\_3, the PMOS input transistors PMOS\_1 and PMOS\_5 and the PMOS control transistors PMOS\_2 and PMOS\_6 are adopted to change oscillation frequency by varying the control voltage  $V_{cont}$ .  $V_{IN1+}$  and  $V_{IN1-}$  represent the differential voltage that is applied to the NMOS input transistors NMOS\_1 and NMOS\_2, and  $V_{OUT-}$  and  $V_{OUT+}$  constitute the differential output voltage of the delay cell.

Due to the oscillation condition of the four-stage structure, the phase difference between the input ( $V_{IN1+}$ ,  $V_{IN1-}$ ) and output ( $V_{OUT-}$ ,  $V_{OUT+}$ ) is  $V_{IN2-}$  and  $V_{IN2+}$  are applied to the PMOS input transistors and PMOS\_5 respectively. As  $V_{IN2-}$  and  $V_{IN2+}$  are taken from a delay cell that is two stages away from the corresponding delay cell,  $V_{IN2-}$  and  $V_{IN2+}$  come  $45^\circ$  earlier in phase than  $V_{IN1+}$  and  $V_{IN1-}$  [7]. The proposed VCO adopts the negative skewed delay scheme reported in [6] for fast transition as a method to improve the phase noise



**Fig-3: Single Delay Cell**

#### IV. SIMULATION RESULT

In this section we present simulation result of four stage ring VCO. We performed spice simulation for proposed circuit by using Tanner EDA software; we use S-Edit, T-Spice W-Edit as a simulator. The supply voltage required for this delay cell is 1V. Low power consumption is achieved by adjusting the supply voltage and input frequency.

##### 3.1 Frequency Tuning Range

In order to validate the proposed circuit in wide frequency range, the simulation is done at different control voltage. It is being seen that if the control voltage is set to 0.2 V the proposed circuit is able to work in 1.06 GHz frequency. While VCRO's control voltage is increased to 0.7 V, the circuit oscillates in 1.17 GHz frequency. It is observed that by increasing the control voltage made the circuit working in higher frequency without changing the oscillation output voltage, i.e., the amplitude remains constant with increasing frequency.

The oscillation frequency is calculated by

$$F_{osc} = \frac{1}{T_d} \quad (7)$$

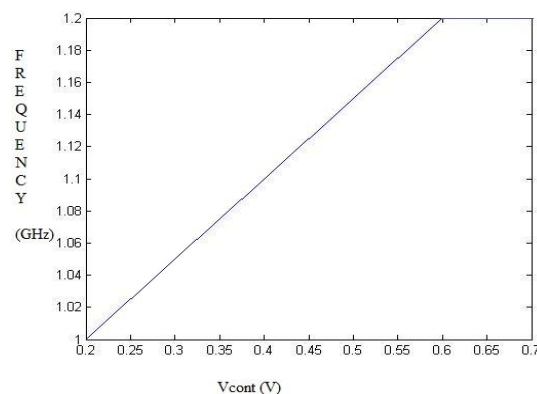
Where,  $T_d$  is the time delay.

The voltage gain of VCO

$$K_{VCO} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \quad (8)$$

The gain of VCRO is achieved 220 MHz/V from (8)

Vcont(V)	Frequency(GHz)
0.2	1.06
0.3	1.10
0.4	1.12
0.5	1.15
0.6	1.16
0.7	1.17



**Fig-4: Voltage Frequency Curve**



### 3.2 Power Dissipation

In order to maximize the output swing, the source nodes of transistors PMOS<sub>4</sub> and PMOS<sub>3</sub> are directly connected to the power supply. At supply voltage V<sub>dd</sub> of 1V, the maximum power dissipation of the ring oscillator was found to be around 8.63 mW which is very small. Fig shows the curve between control voltage and power dissipation.

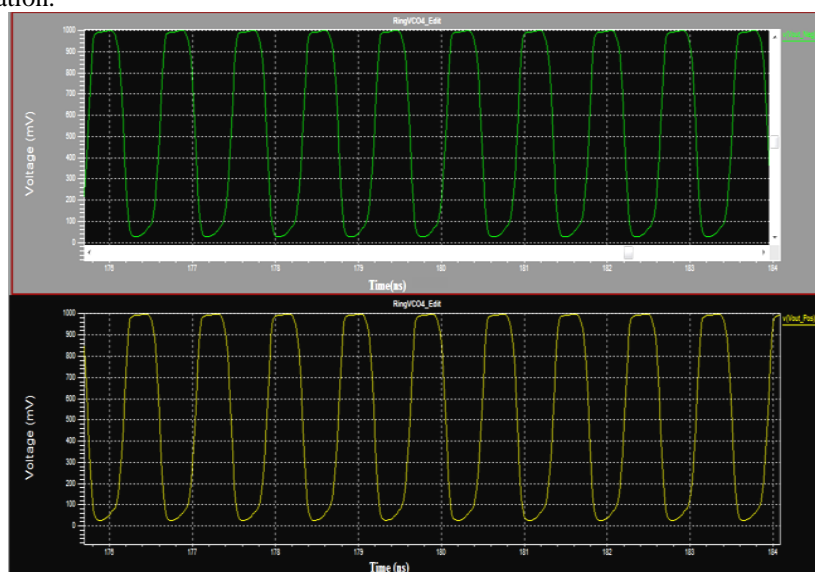


Fig-5: Simulated Result of proposed Ring VCO

## IV. ANALYSIS OF RESULT

Table I shows the performance comparison of different VCO architecture with different design parameters and the different technology. As shown in table I [4],[5] and [6] where designed on 180nm CMOS technology. The power dissipation obtained is more compared to proposed work. Joo-Myoung Kim [1] worked on 65nm CMOS technology reports good performance of phase noise -110dBc/Hz at low voltage 1V but at low frequency tuning range.

The proposed ring VCO operates at frequency range 1.06-1.17GHz which high as compare to design shown in [1] which is having frequency tuning range 0.645-1.10GHz. The power dissipation obtained in [1] is 10mW, 13mW in [4] while in proposed work power obtained is 8.63mW which is less compare to previous work. The design [4] is working with high frequency but power dissipation is more. We achieve the low phase noise with respect to the previous designs; this is most important benefit of work.

TABLE I: PERFORMANCE COMPARISONS OF CMOS VCRO

Sr. No.	References	Technology(nm)	Supply Voltage(V)	Pdiss(mW)	Frequency(GHz)	Phase Noise (dBc/Hz)
1	[5]	180	1.8	11.39	186-1.25	-101
2	[6]	180	1.8	39	1.4	NA
3	[4]	180	1.8	13	1.77	-102
4	[1]	65	1	10	0.645	-110
5	<b>This Work</b>	65	1	8.63	1.17	-101

## V. CONCLUSION

Voltage Controlled Oscillator schematics is designed and simulated using Tanner Tool version 13.0 in a 65nm CMOS technology library. The performance of circuits is evaluated in spice simulation by using T-spice simulator in a 65nm CMOS technology. The proposed work achieves the better results of performance parameters such as oscillation frequency and power consumption compare to previous work. The proposed ring VCO is implemented in 65-nm CMOS technology, supply voltage is 1V. The VCO consists of four stage fully differential delay cells, which uses transmission gates control delay. Simulation results show that the VCO can operate from 1.06GHz to 1.17GHz by varying control voltage from 0.2V to 0.7V. Oscillation frequency at supply voltage 1V is obtained 1.17GHz, power dissipation is 8.63 mW and phase noise obtained is -101dBc/Hz. The proposed VCO can be used for wide tuning application and low power consumption.

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