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POWER EFFICIENT ENHANCED DUAL DYNAMIC HYBRID FLIP-FLOP

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ABSTRACT

In this paper, we introduce a new dual dynamic hybrid flip-flop with self controllable voltage level circuit (DDFF-SVL).The proposed techniques are eliminate large area penalty large power penalty due to substrate-bias supply circuits and very slow substrate-bias controlling operation. This designs also eliminates large capacitance present in the precharge node of several state of the art designs, following the split dynamic node structure, that separately drives the output pull-up and pull-down transistors. The proposed designs are reduce power dissipation, delay and area. The performance comparisons made in 0.18um technology using mentor graphics tool. The speed remains almost constant in terms of the switching the input signal by adding "self-controllable voltage level circuit(SVL).The result of the simulation shows that this DDFF-SVL circuit is a viable to improve the performance and it achieves greater power efficiency.

KEYWORDS: *SVL Circuit, Embedded logic, flip flops, low power, high speed*

1. INTRODUCTION

Very Large Scale Integration (VLSI) describes about semiconductor integrated circuits which composed of hundreds of thousands of memory cells logic elements.In synchronous systems high speed has been exploitation advanced of all pipelining techniques. In new deep pipelined architectures increases the speed and up demands of a pipeline overhead. Thattype of overhead is latency, it is related to the pipeline elements like flip-flops and latches. Flip-flop[2] and latch are the two basic building blocks of a sequential circuit.

A recent paper introduced hybrid latch flip-flop (HLFF)[3] and semi dynamic flip-flop (SDFF)[4].These two flip -flops are classic high performance flip- flops. Hybrid latch flip flopis one of today's high performance flip –flops. It minimizes clock skew but it has large power consumption.SDFF has capability of incorporating logic very efficiently because unlike the true single phase latch (TSPC) This is very useful in reducing the pipeline overhead. Hybrid latch flip-flops designs proposed all timing at reducing the power, area and delay.SDFF is capable of offering efficiency in terms of speed, area it is not good solution as far as power consumption is concerned.

In this paper a low power and high-speed flip-flop named cross charge-control flip-flop (XCFF)[6]. one of the major draw backs of this design is the redundant precharge at notes for data patterns.XCFF combines the advantages of both power and speed in HLFF and SDFF.But it has the problem for degradation of the speed. low power and high-performance flip-flops namely conditional data mapping flip-flops (CDMFFs)[5].Which reduce the dynamic power by mapping there inputs configuration that eliminates redundant internal transitions. This flip flop having charge sharing problem because of the uncontrollably large when complex functions are embedded into the design.

Dual dynamic flip-flop (DDFF)[1]and dual dynamic flip-flop with embedded logic module (DDFF-ELM)[1].Both eliminate drawbacks of XCFF.These two designs are eliminate when the large capacitance present in the precharge node of several state- of -the art design of the split dynamic node structure separately use the output pull up and pull down transistors. DDFF gives power reduction and high speed, low power .The other method DDFF-ELM presents speed, area and power efficientmethodto reduce the pipeline overhead.

In this paper we proposed Dual Dynamic node hybrid flip-flop with self controllable voltage level circuits (DDFF-SVL), and DDFF-ELM with SVL.The speed remains almost constant in terms of the switching input signal by adding Self -controllable voltage level circuit(SVL).This SVL circuit improve the design performance, achieve high power efficiency and low power The performance of all high performance flip-flops are compare with these flip-flops at different data activities. The simulation results in 180 nm UMC process.

The rest of the part of this paper divided as follows. Section II describes flip-flop architecture and operations the disadvantages of all the existing flip-flops. In Section III, The proposed DDFF-SVL and DDFF-ELM-SVL architecture and operation are provided. Section IV performance analysis of all methods to compare the proposed flip-flop architectures. Section V It includes technology parameters used for simulation. Section VI the results of various performances including power, area, delay, risetime, falltime are provided.Section VII finally we conclude the improvements of the proposed flip-flop designs over the existing high performance designs.

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2.ANALYSIS OF FLIP-FLOP ARCHITECTURES

The Power PC 603 flip-flop(fig.1)[2] has a structure and it is the combination of TGMS flip –flop and mC2MOS Flip-Flop. This PPC flip-flop realized by using two transmission gates based latches operating on complimentary clocks. The feedback transmission gate is also changed with clocked inverter.

PowerPc 603 is one of the most efficient classic static structure. advantage of this flip-flop low- power keeper structure and low latency direct path. Disadvantage of this design large data and clock node capacitance in performance.

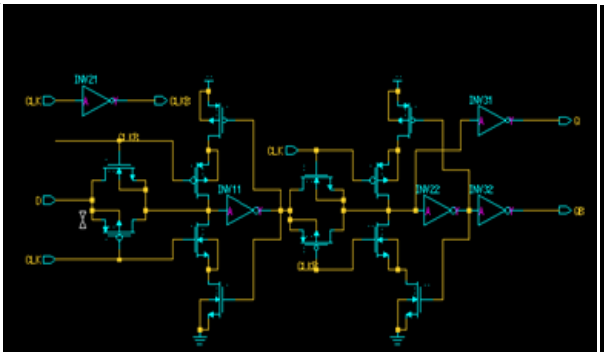

Fig.1.POWER PC 603 FLIP-FLOPS

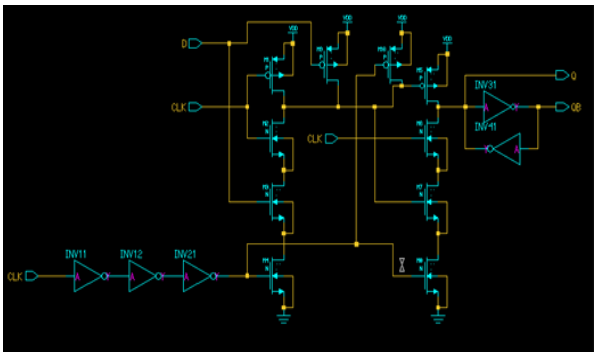

Fig.2. HYBRID LATCH FLIP-FLOP

The second category of flip-flop the hybrid latch flip-flop (HLFF)(fig.2)[3]it introduces new mechanism of performance flip-flop functionality. The ideal input signals are 0 to 100% rise and falltimes.Once all the constraints are achieved is to minimize the total power consumption. Advantage of this flip-flop it minimizes the clock skew but it has large power consumption.

The third category of the flip-flop is semi dynamic flip-flop(SDFF)[3]. It is the fastest classic hybrid structure but it is not different in terms of power consumption because of large CLK load. This flip-flop having both the advantages and disadvantages. Greatly reduces pipeline overhead, it is capable of offering the efficiency interms of speed and area it is not good solution as far as power consumption is concerned.

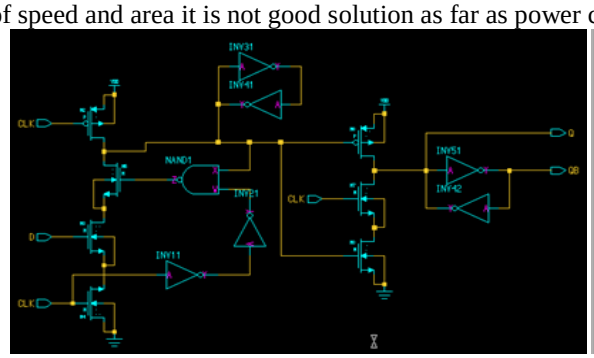

Fig.3.SEMI DYNAMIC FLIP-FLOP

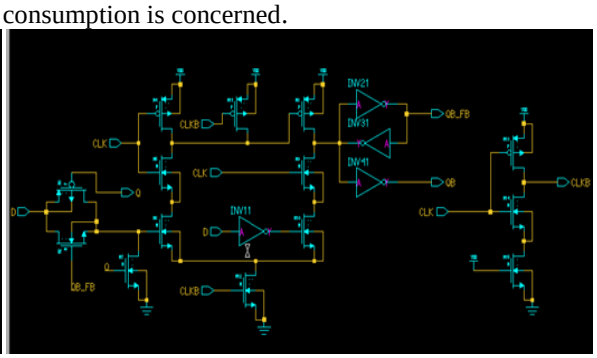

Fig.4.CONDITIONAL DATA MAPPING FLIP-FLOP

Fourth category of the flip-flop is conditional data mapping flip-flop(CDMFF)(fig.4)[5] it is one of the most efficiant flip-flop.it reduce the dynamic power by mapping their inputs to a configuration that eliminates Redundant internal transitions. increasing power dissipation at higher data activities.it reduces total power dissipation but it has charge sharing problem because of unconrollably large when complex functions are embedded into the design.

Fifth category of the flip-flop is cross charge control flip-flop (XCFF)(fig.5)[6].It reduces the power dissipation by splitting the two dynamic nodes into two each one seperatly driving the output pullup and pulldown transistors.It combines the advantages of both power and speed in HLFF and SDFF.but it has the problem for degradation of the speed.

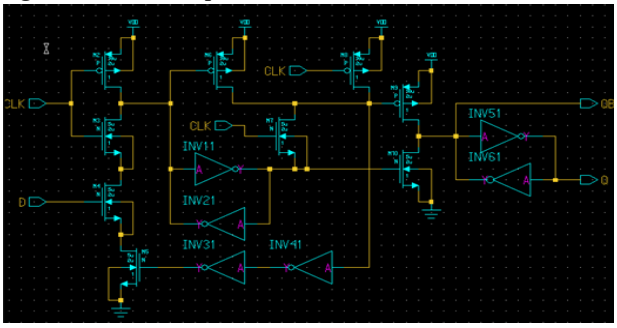

Fig.5.CROSS CHARGE CONTROL FLIP-FLOP

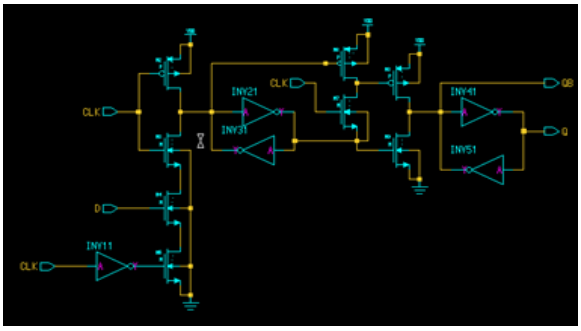

Fig.6.DUAL DYNAMIC FLIP-FLOP

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Sixth category of the flip-flop is Dual Dynamic lip-flop(DDFF)(fig.6)[1].This designs are eliminate the large capacitence present in the precharge node of the several state-of-the art designs by following splitt dynamic structure drive to seperatly the output pullup and pulldown transistors..it can achieve high performance but it has power consumption.
Seventh category of flip-flop is Dual Dynamic flip-flop with embedded logic module(DDFF-ELM)(fig.7)[1]. It performs the function of flip-flop when no logic is embedded its performance of a flip-flop is compared with other flip-flops along with DDFF . flip-flop performing the same functions..by using the technique we can reduce power and achives high speed operation through pipeloning function and area and delay decrease.

3.PROPOSED DDFF-SVL AND DDFF-SVL-ELM ARCHITECTURES

Design techniques for all low power circuits are not only needed for logic circuits but also for storge circuits,they are flip-flops register files and memorys .there are two important techniques for reducing standerd - by power.

I.Multi threshold voltage CMOS(MT CMOS)
II.variable threshold voltage CMOS(VTCMOS)

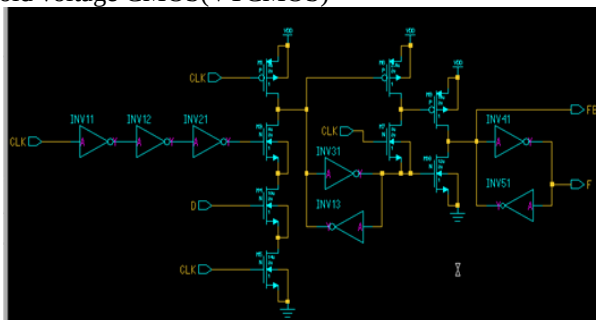

Fig.7.DUAL DYNAMIC FLIP-FLOP WITH EMBEDDED LOGIC MODULE

In this First technique MTCMOS reduces Pst by disconnecting the power supply through the use of P-MOSFET switches with higher threshold voltage it has seviour draw backs such as need for additional fabrication process for higher Vth and the fact storage ciecuits based on the technique can't retain data.In Second technique reduces leakage current.But in this technique also faces serious problems they are very slow substrate-bias controlling operation,large power penalty due to substrate-bias supply circuits,large area penalty.
To solve above draw backs we use self controllable-voltage-level (SVL)(fig.8) circuit.In this circuit significantly decrease Pst while maintaining high speed performance.The SVL circuit consists of an upper SVL(U-SVL) and lower SVL(L-SVL) circuit.In dual dynamic node hybrid flip-flop has been used as the load circuit.The upper SVL consist of single P-MOSFET switch (P-SW) and m n-MOSFET switches (n-SW), and the lower SVL circuitconsist of single n-MOSFET switch (n-SW) and m p-MOSFET switches connected into series.
The "on p-SW" connects power supply Vdd and load circuit in active mode and "on n-SW" connects VDD and load circuit in standby mode.same as the lower SVL circuit consists of single n-MOSFETswitch(n-SW) and m p-MOSFET switch connected in series it is located between the ground level and load circuit the lower SVL not only supply Vss to achiev load circuits the "on n-SW" but it supplys Vss to standby load circuit use of on p-SW.where the load circuit is active both the p-SW and n-SW are turned into on.but the nRSI & pRSI are turned into off.then the upper SVL and lower SVL circuits are supply maximum supply voltage (VD=VDD) and minimum ground level voltage (VS=VSS=0) to the active load circuit then the operating speed of the load circuit can be maximize.

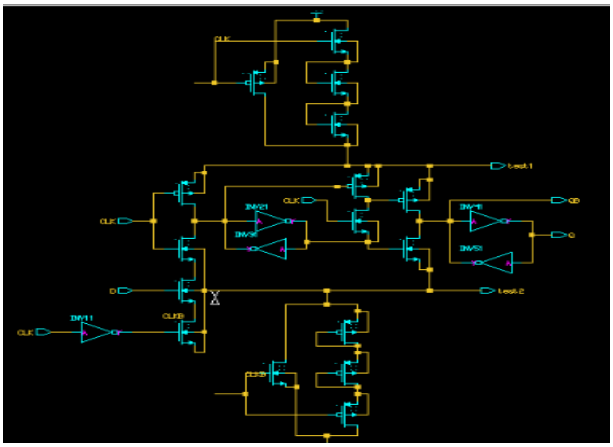

Fig.8.DUAL DYNAMIC FLIP FLOP WITH SVL

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4. RESULTS AND COMPARISONS

The results are comapared with the existing technique the tablation of performance comparison of the proposed existing techniques is shown bellow(Table.1).The area of proposed design has got comparatively increases with the existing designs.power dissipation of the existing design has got decreases comapared to the proposed technique.risetime and falltime values are also give the better results compared to the proposed techniques.the current value is also reduced efficiently in the proposed method.the results of DDFF-SVL & DDFF-ELM-SVL are compared with existing methods it proves to be better than the existing methods.

Table.1.Performance comparision of various Embedded functions

FLIPFLOP	RISE TIME(ns)	FALL TIME(ns)	DELAY(ns)	DYNAMIC POWER(µW)	STATIC POWER (pW)
POWER PC	7.398	9.766	22.087	90.361	387.73
HLFF	5.858	3.379	27.164	81.316	234.04
SDFF	3.745	2.562	25.594	87.591	291.05
CDMFF	8.076	8.041	24.576	85.276	254.78
XCFF	4.221	1.942	28.276	89.576	304.89
DDFF	1.352	1.101	25.940	78.962	220.15
DDFF-ELM	8.712	5.018	26.798	78.362	263.66
DDFF-SVL	1.344	0.586	17.880	76.926	218.13

180-nm UMC transistor mode is used in the simulation process. The supply voltage of the model is 1.8V.measurements are made at different PVT conditions.the power is found as the difference between power dissipated inverter when loaded with the flip-flop and not loaded with flip-flop.The risetime is calculated at the rise edge of the output,the falltime is also calculated fall edge of the output.

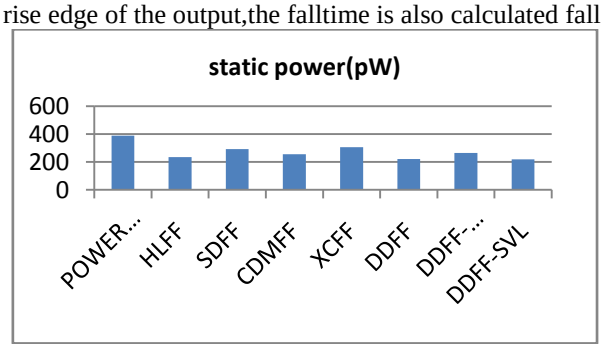

Fig.10.static power comparision

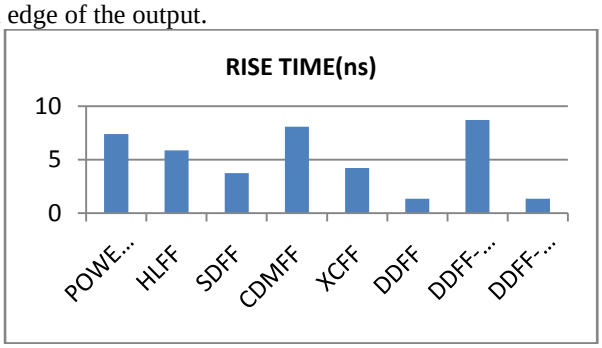

Fig.11.Rise Time comparison

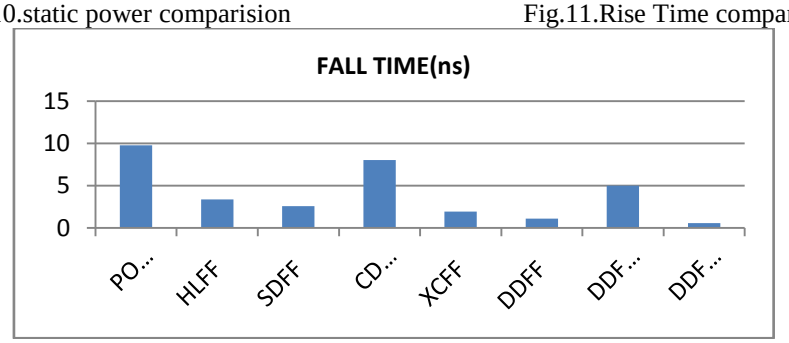

Fig.12.Fall time comparision

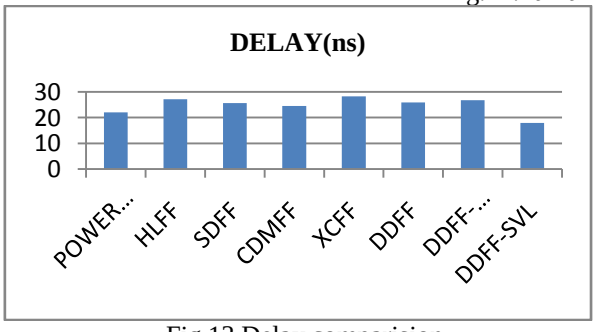

Fig.13.Delay comparision

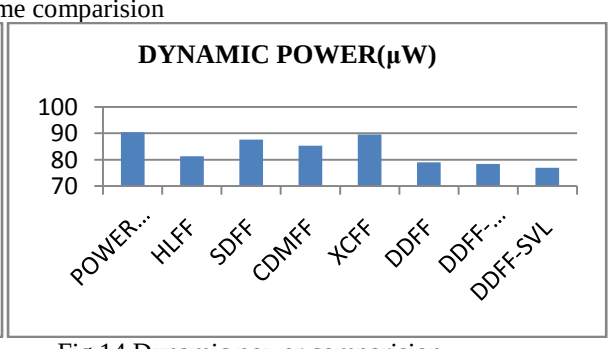

Fig.14.Dynamic power comparision

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CONCLUSION

In this paper a new low power DDFF-SVLare proposed.the proposed technique eleminate large area penalty large power panalty due to substrate-bias supply circuits and very slow substrate-bias controlling operation.A comparision of the proposed flip-flop with the conventional flip-flops exhibits lower power dissipation along with comparable speed performances.this SVL circuit consist of 3 moduels upper level SVL circuit controls Vdd lower level circuit controls ground and DDFF acting as load circuit.DDFF-SVL considered as best logic design style compared to all other existing flip-flop.DDFF-SVL lowest power dissipation and comparable propagation delay by using SVL circuits.

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