Vol 05, Article 09449, October 2014 International Journal of VLSI and Embedded Systems-IJVES
http://ijves.com ISSN: 2249 – 6556

LOW POWER CURRENT COMPARISON DOMINO LOGIC FOR WIDE FAN IN GATES

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ABSTRACT

In recent years power saving is one of the important thing. Domino logic circuit is power efficient cicuit,so it is widely used in variety of applications in digital design. But it has a limitation of low noise immunity and more leakage current. This problem can be solved by using keeper transistor to compensate leakage current of pull down network. The conventional keeper domino circuit reduces the performance and more power consumption due to the contention between keeper transistor and pull down network. This problem is more in wide fan in OR gates due to large number of leaky paths connected to the dynamic node. In this paper ,a new technique is proposed which overcomes the contention problem and reduces power dissipation and provide high noise immunity. Simulations of wide fan in OR gates are designed using TSMC 180nm technology with Vdd=1V at 27⁰ c and 110⁰ c demonstrate 50% power reduction using mentor graphics.

Keywords : *Domino logic,dynamic node,wide fan in,noise immunity.*

1.INTRODUCTION

Static cmos logic circuits with complementary NMOS pull down and PMOS pull up networks are used for the majority of logic gates in integrated circuits.static gates have limitations, area and speed especially for wide fan in gates. To overcome these issues ,we can go for pseudo NMOS logic gate, which are most common form of CMOS ratioed logic.pull down network is same like that of static cmos logic gate ,but the pull up network is replaced with single PMOS transistor that is grounded so it is always ON. Pseudo nmos logic circuit has a limitation of static power dissipation and weak low level at output. By combining the advantages of low power from static cmos logic and less area from pseudo nmos logic the dynamic logic circuit is formed by introducing the clock input signal. Dynamic cmos logic required number of transistor that is for fan in n is n+2. Dynamic circuit reduces the short circuit power dissipation. But dynamic logic suffers from charge sharing,charge leakage and clock skew.dynamic circuit sharing the same clock cannot be directly connected . these problems are overcome with domino logic.Domino logic circuits with high fan in gates are widely used due to their high performance.Domino logic circuit is formed by adding a static CMOS inverter to the output of dynamic CMOS logic. The idea of forming domino logic is to limit charge leakage and charge sharing by feeding back the inverting output. Major drawback of domino logic circuit is more sensitive to noise than static logic families.. On the other hand, Power consumption is one of the important factor in present days especially for portable devices.one way to achieve low power is scaling down the supply voltage.as supply volge reduce, the threshold voltage(vth) of transistors are reduced.however lowering he threshold voltage leads to an exponential increse of suthreshold leakage current. Another way to reduce power is technology scaling,as the technology scales down in nano meter technology,the gate oxide thickness is scaled down. Such thin gate oxide leads to significant gate leakage current ecause of enhanced tunnelling of carriers. For these reasons static power consumption i.e, leakage power dissipation , has become a dominant factor for current and future technologies.Reduction of leakage current and improving noise immunity is a major concern.

These issues can be solved by employing PMOS keeper transistor in standard footer less domino logic Schematic of basic standard footerless keeper domino shown Fig 1. that compensates leakage current of pull up network. Keeper ratio defined as the ratio of the current drivability of keeper transistor to the evaluation network.

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{\text{keeper transistor}}}{\mu_n \left(\frac{W}{L}\right)_{\text{evaluation transistor}}}$$

Operation of domino logic occurs in 2 phases.In Precharge phase, clock signal is at low i.e,(clock =0) all the inputs at low,the dynamic node pulled up to Vdd through Precharge PMOS device. In evaluation phase, clock signal is at high i.e,(clock =1) depends on input pattern either charge of dynamic node retained or removed. If all the inputs at low,output of OR gate must be zero,hence dynamic node must remain high and consequently the pmos keeper must stay on to compensate for any leakage current drawn out of dynamic node. In the case where atleast one of the input is high, stored charge on dynamic node must be discharged. In this case both pmos and keeper transistor and pull down network circuit simultaneously ON during the time interval from when pull down network starts conducting until voltage of output node reaches a certain high voltage.the contention etween keeper and pull down network increases bothdelay and power

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http://ijves.com ISSN: 2249 – 6556

consumption.un the case strong keeper,desirable to increase noise margin.while weak keeper is to increase speed up switching transistion. There is conflict requirement gives rise to tradeoff between power and performance.

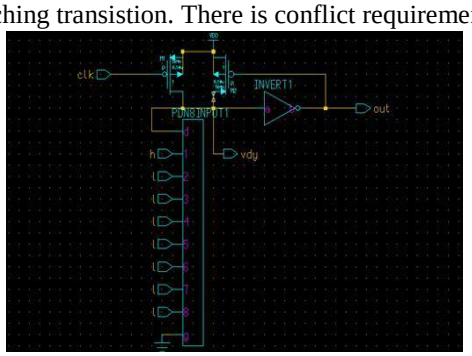

Fig 1: standard footerless domino logic (SFLD)

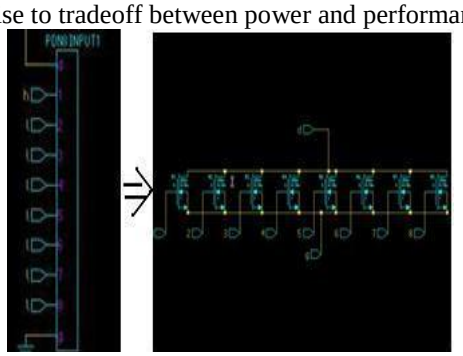

Fig 1.1: Pull down network

2. LITERATURE SURVEY OR PREVIOUS WORKS

Several domino techniques have been proposed in the literature such as conditional keeper domino logic (CKD) [2], diode footed domino logic (DFD)[3], leakage current replica keeper logic (LCR)[4], controlled keeper by current comparison domino logic (CKCCD)[5] are shown in fig 2.1,2.2,2.3,2.4, respectively. The main goal of these circuits is to reduce leakage and power consumption and improve noise immunity,especially for wide fan in gates.

2.1 Conditional Keeper Domino Logic (CKD):

One of the existing domino logic is conditional keeper domino (CKD) logic[2] shown in figure.Conditional keeperdomino logic circuit consists of 2 keeper transistors,small keeper andlarge keeper transistor.

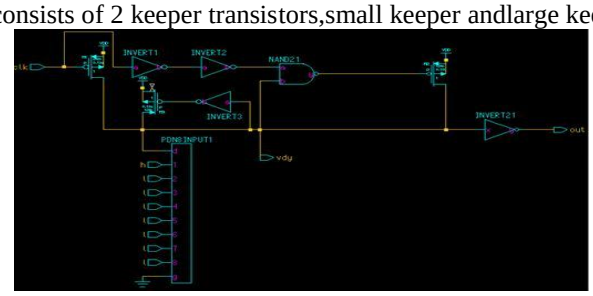

Fig 2.1 conditional keeper domino (CKD) logic

Circuit operates as follows: In precharge phase when clock is low,the pull up transistor is on ,so the dynamic node charged to Vdd. At the beginning of evaluation phase when clock is high,the small keeper K1 turns on to hold the state of the dynamic node and large keeper k2 turns off for some time. If the dynamic node still high after the delay of two inverters, the output of the nand gate goes low and turns on the keeper transistor K2. This keeper transistor sized larger than keeper transistor K1 to maintain the state of dynamic node for the rest of evaluation phase to improve the robustness of the circuit. However, conditional keeper domino has some drawbacks such as increasing delays of the inverters and nand gate to improve noise immunity to the circuit.

2.2 Diode Footed Domino (DFD):

In diode footed domino logic [3], NMOS transistor m1 connected in diode configuration i.e, gate and drain terminals are connected together in series with the evaluation network. Diode footer m1 reduces sub threshold leakage current due to the stacking effect. Due to the leakage current of evaluation transistors, there is some voltage established across diode footer m1 in the evaluation phase. This voltage drop makes Vgs of the off evaluation transistor negative, causing an exponential reduction in sub threshold leakage. Voltage drop across diode footer increases the body effect of the evaluation transistor which also helps in reducing the sub threshold leakage. on the other hand diode footer transistor m1 increases the switching threshold voltage of the gate by the threshold of nmos devices and hence gate switching vth is 2vth. higher switching voltages results better noise immunity.

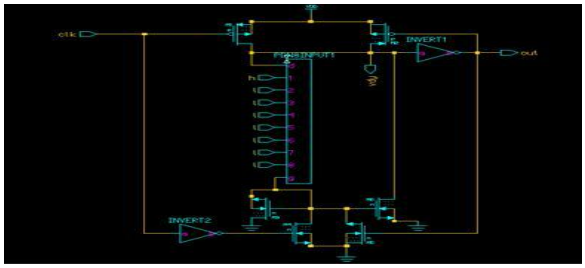

Fig 2.2: diode footed domino (DFD) logic

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2.3 Leakage Current Replica Keeper (LCR)

In leakage current replica keeper [4], current mirror circuit is added to the keeper of standard footer less domino logic. Transistor m1 of the mirror circuit is connected in diode configuration, i.e, gate of the pmos transistor is connected to the drain. By doing like this both gate and drain of the pmos transistor is at potential voltage level of the keeper. Keeper voltage is same as the potential of drain of keeper transistor mk1. This leakage current replica keeper reduces the power consumption .

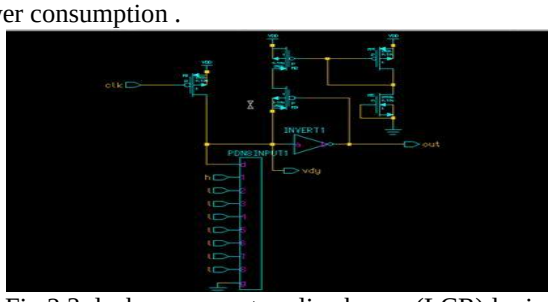

Fig 2.3: leakage current replica keeper(LCR) logic

Operation of circuit is as folllows : In precharge phase, when clock is low and all the inputs are at low level , dynamic node charged up to Vdd. During precharge phase, output is at low which turns on the keeper transistor MK2 and it acts as a short cuircuit transistor. Now the drain of MK1 transistor is directy connected to the dynamic node and due to the diode configuration of this keeper transistor MK1 drain voltage of M1 is also at the logic low level of dynamic node. High voltage of drain of M1 transistor reduces the eakage current. In this way, the leakage power is reduced.

2.4 Controlled Keeper By Current Comparison Domino (CKCCD)

In CKCCD technique, keeper transistor controlled by the current comparison domino mechanism. Basic idea of this technique is that keeper transistor is controlled with the current comparison so that when dynamic node is truly discharged, keeper transistor will be off to prevent the contention between keeper transistor and pull down network. Due to this power and the propagation delay gets reduced.

Schematic of CKCCD shown in fig 2.4, in this circuit M1 added in series with the evaluation network which is connected in a diode configuration to provide more leakage current reduction when all the inputs in the OR gate at the low level or in standby mode.

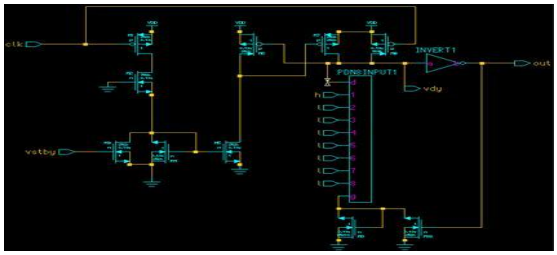

Fig 2.4: Controlled keeper by current comparison domino (CKCCD) logic

Circuit operates as follows: In Precharge phase, when clock is in low level i.e,CLK= ‘0’.so the precharge transistor Mpre , keeper Mkeeper and M8 are on and M1 and M2 are off. Then the voltage of the dynamic node is raised to high level by the transistor Mpre. In this phase ,leakage current is reduced due to the stacking effect because the minimum voltage of a MOS transistor in diode configuration is identical to vgs=vds=vtn.

In Evaluation phase , when clock is in high level i.e, CLK=’1’. So the precharge transistor and M8 are off. According to the mirror current and discharge current of pull down network, two states might possible . Depending on the inputs, other transistors may be turns on or off. First if all inputs at low level, the mirror current is larger than the PDN leakage current, the voltage node is discharged to zero. Then, the keeper transistor is turns on and maintains the dynamic node at a high level. Second , if atleast one of the inputs at high level, the discharging current of PDN is larger than the mirror current, give up the voltage if node remains high. This reduces the contention by turning off the keeper transistor.

3. PROPOSED WORK

Current Comparison Domino Logic (CCD) Logic:

In case of wide fan in gates, capacitance of the dynamic node is large then speed decreases severely. Due to the large parallel leaky paths, power consumption increases and noise immunity reduces. These problems will be solved if pull down implements logic function is divided from keeper transistor by comparison stage in which current of pull up network compared with the worst case leakage current.

Circuit operates as follows:

Pre discharge Phase: When CLOCK is at low level i.e, CLK=’0’ and all input signals are at high level . in this phase, voltage of the dynamic node have fallen to low level by the transistor Mdis and raised to high level by the

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transistor Mpre. Therefore, the transistors Mpre, Mdis, Mk1,Mk2 are on and other transitors are off. Then the output voltage raised to high level.

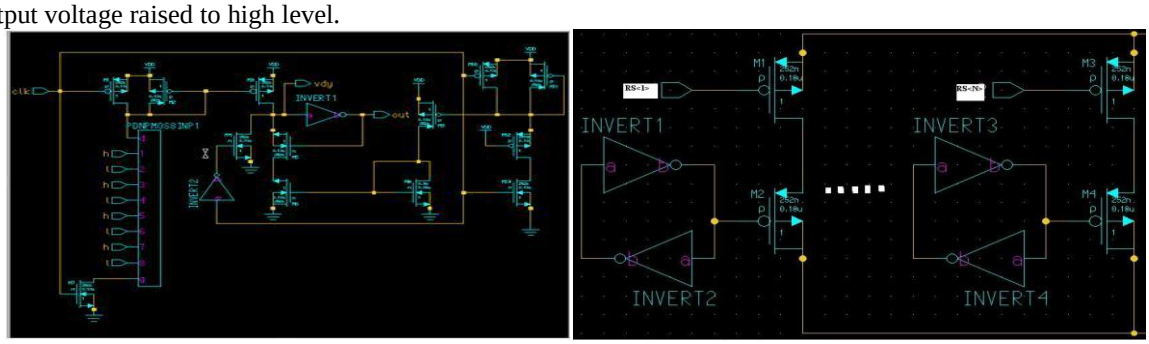

Fig 3: Wide Fan In OR Gate Using Current Comparison Domino (CCD) Logic
Fig 4: local bit line scheme in pull down network

Evaluation phase: When CLOCK is at high level CLK='1' and the transitors may be turns on or off dependin on the input voltages.here two states may possible, first all the inputs are high, a small amount of voltage is recognized across the transistor M1 due to leakage current. Even though the leakage current is mirrored by transistor M2, the keeper transistor of the second stage Mk1 and Mk2 give back this mirror leakage current. It is clear that upsizing transistor M1 and increasing the Mirror ratio increases the speed at cost of high noise immunity degradation. Second ,at least one input falls to low level, one conduction path exists, pull up current flow is raised and voltage of node is reduced to non zero voltage, which is equal to the gate source voltage of the saturated transistor M1. This voltage same as the drain to source voltage of M1 depend on size of M1 and its current. Increasing the pull up current increases the mirrored current in transistor M2, thus voltage of the dynamic node is charged to Vdd, yields discharging the voltage of the output node and turning off the main keeper transistor Mk1.due to this contention between keeper and mirror transistor are mitigated.

4. SIMULATION RESULTS AND COMPARISONS

The proposed circuit simulated using mentor graphics in the TSMC180nm technology in the 27⁰ c and 110⁰ c and the supply voltage used in the simulations is 1V.table1 and table 2 shows power dissipation at 27⁰ C and 110⁰ C comparison between SFLD and various domino logics.

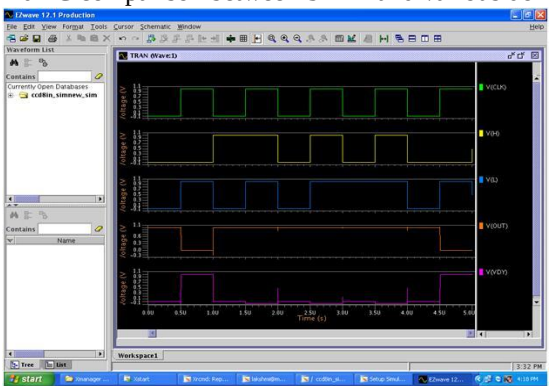

Fig.4.1 shows output of OR gate using CCD

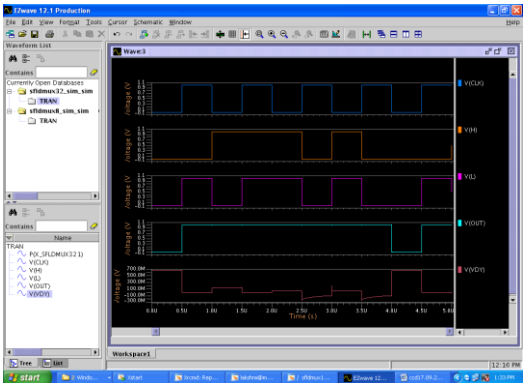

Fig.4.2 shows output of MUX using SFLD

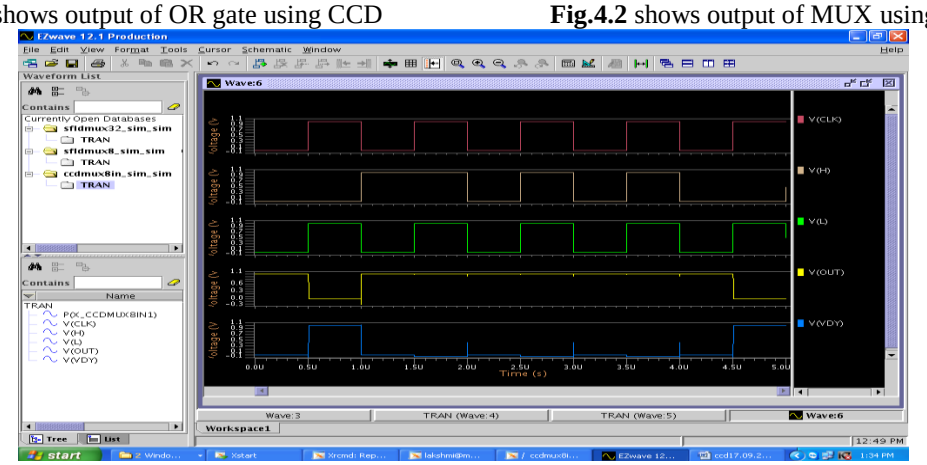

Fig.4.3 shows output of MUX in local bit line scheme gate using CCD

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Table 1 comparison of Power Dissipation (Pw) at 27^{0C} Temperature between various domino logics

FAN IN	PARAMETER	SFLD	CKD	DFD	LCR	CKCCD	CCD
8	POWER	67.94	82.4	75.03	7528	38.78	33.75
8	NORMALIZED POWER	1	1.21	1.1	1.1	0.57	0.49
16	POWER	118.38	139.75	133.43	132.78	51.56	34.98
16	NORMALIZED POWER	1	1.18	1.12	1.12	0.43	0.29
32	POWER	233.163	254.76	248.13	283.65	76.52	35.87
32	NORMALIZED POWER	1	1.09	1.06	1.21	0.32	0.13
64	POWER	463.16	484.72	478.72	549.18	108.2	36.69
64	NORMALIZED POWER	1	1.04	1.03	1.18	0.23	0.07

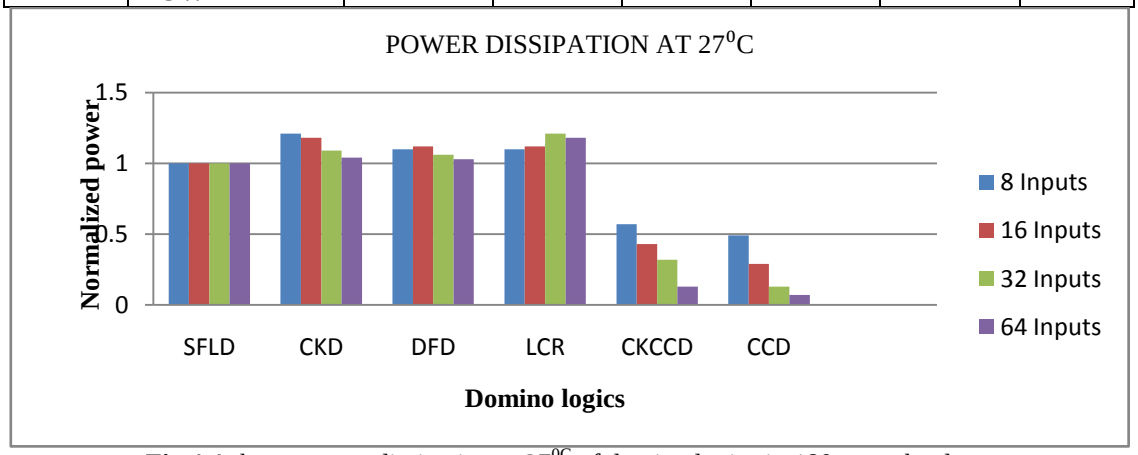

Fig.4.4 shows power dissipation at 27^{0C} of domino logics in 180nm technology

Table 2 comparison of Power Dissipation (nw) At 110^{0C} between various domino logics

FAN IN	PARAMETER	SFLD	CKD	DFD	LCR	CKCCD	CCD
8	power	5.36	7.41	6.37	5.90	5.64	3.37
8	Normalized power	1	1.38	1.18	1.10	1.05	0.62
16	power	9.86	12.08	11.04	10.58	9.58	3.37
16	Normalized power	1	1.22	1.11	1.07	0.97	0.34
32	power	19.21	21.43	28.38	20.49	19.10	3.38
32	Normalized power	1	1.11	1.47	1.06	0.99	0.17
64	power	37.90	40.12	39.05	39.76	33.27	3.39
64	Normalized power	1	1.05	1.03	1.04	0.87	0.08

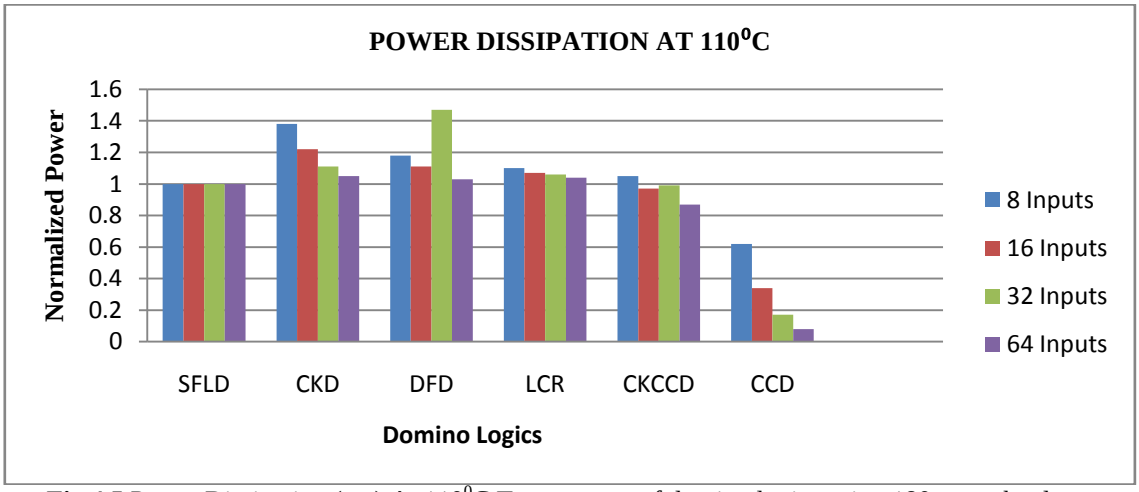

Fig 4.5 Power Dissipation (nw) At 110^{0}C Temperature of domino logics using 180nm technology

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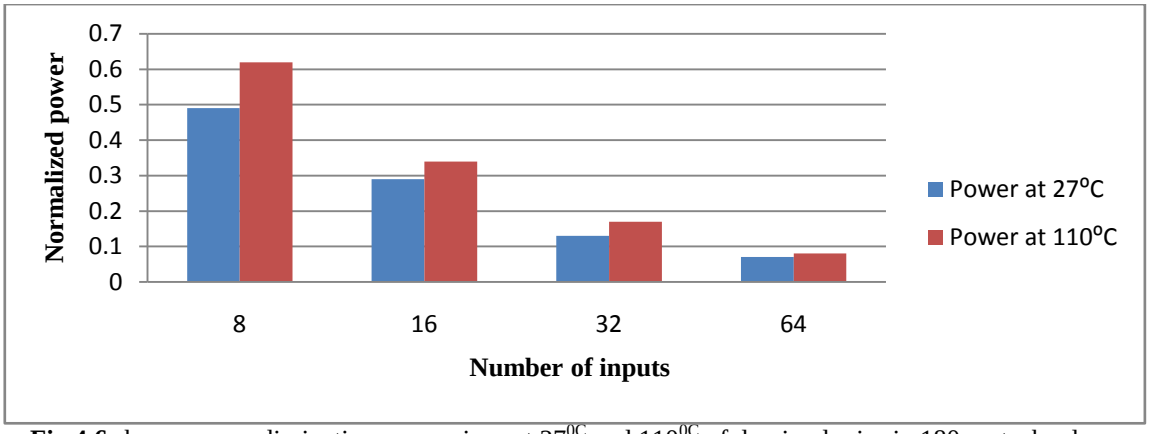

Fig 4.6 shows power dissipation comparison at 27^{0C} and 110^{0C} of domino logics in 180nm technology

So, Proposed circuit CCD has less power dissipation compared to the SFLD as the temperature and number of inputs increases.

Table 3 comparison of Power Dissipation between wide OR gate using SFLD, CCD and MUX in local bit line (LBL) scheme using SFLD and CCD

FAN IN	PARAMETER	SFLD OR GATE	SFLD MULTIPLEXER	CCD OR GATE	CCD MULTIPLEXER
8	POWER	67.94pw	135.32pw	33.75pw	116.07pw
16	POWER	118.38pw	26.08 µw	34.98pw	200.13pw
32	POWER	233.16pw	40.58 µw	35.87pw	367.32pw
64	POWER	463.16pw	42.98 µw	36.69pw	698.34pw

Table 4 comparison of delay between various domino logics

FAN IN	PARAMETER	SFLD	CKD	DFD	LCR	CKCCD	CCD
8	DELAY	498.41	0.545	498.48	499.77	39.05	501.35
16	DELAY	0.573	0.626	0.578	0.553	17.18	501.35
32	DELAY	999.4	499.81	0.112	499.68	4.46	501.35
64	DELAY	0.979	1.07	502.20	974.9	500.08	501.35

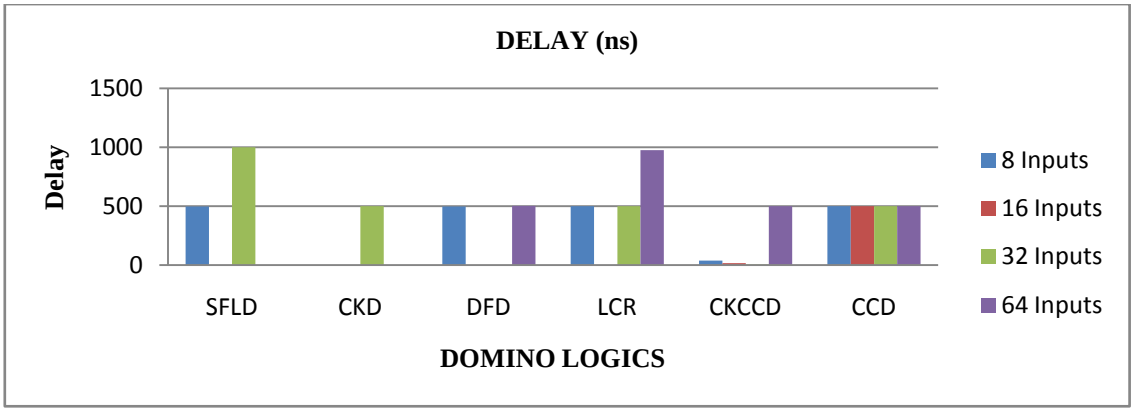

Fig.4.7 shows delay of domino logics using 180nm technology

5. CONCLUSION

Leakage current of the pull down network increases significantly with the technology scaling and reducing supply voltage especially for wide fan in gates. Along with this yields low noise immunity and more power consumption. In addition, increasing fan in not only increases delay, also increases contention between keeper transistor and pull down network. In this, new domino technique called domino technique which increases noise immunity and reduce contention and power dissipation. Existing domino techniques are simulated with mentor graphics in the TSMC 180nm technology at a power supply of 1V.Results of simulations shows that the proposed circuit exhibits less power dissipation for 8, 16, 32 and 64 inputs compared to SFLD.

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