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LOW-POWER, LOW-TRANSITION TEST PATTERN GENERATOR IN LOGIC BIST SCHEMES

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ABSTRACT

In this paper an algorithm is proposed to design a Low power-Test pattern generator (LP-TPG) also called as Modified-Test pattern generator (M_TPG) and a modified Built-in-self-test (BIST) controller for testing ISCAS-85 c432 combinational benchmark circuit. The M_TPG consist of a modified linear feedback shift register and R-injector circuit. The modified linear feedback shift register generates random patterns reducing the switching activity between the successive test vectors by increasing the correlation between them. The proposed algorithm uses the R-injector circuit to provide the 3-intermediate test vectors which effectively increases the correlation between the two successive test patterns thus resulting in reduction of switching activity of the circuit under test (CUT). The Conventional linear feedback shift register is used to generate test patterns in Multiple Single Input Change (MSIC-TPGs) for Test-per-clock (TPC) and Test-per-scan (TPS) BIST schemes, which is then replaced by this proposed LP-TPG, which substantially reduced the dynamic power dissipation of CUT to 21% in TPC and 12 % in TPS schemes attaining the correlation between the successive vectors. Verilog HDL is used as HDL language. The results were analysed using modelsim for simulation and Xilinx for synthesis and is implemented on the field programmable gate array (FPGA) spatan3E hardware..

Keywords: *CUT, MSIC-TPGs, R-injector, LP-TPG, c432 benchmark circuit, TPC, TPS.*

[1] INTRODUCTION

Low Power consumption has become increasingly important in portable devices and wireless communication systems and battery operated equipment, such as laptop computers, audio and video-based multimedia products, and cellular phones. As the reduction of the energy consumption is becoming one of the most growing topics of interest in the electronics industry and one of the most challenging areas of research in this domain. For this a new class of battery- powered devices, the energy consumption is a critical design issue since it determines the lifetime of the batteries. Minimising the power dissipation in VLSI circuits increases battery lifetime and the reliability of the circuit. The power dissipation of complementary metal oxide semiconductors (CMOS) circuits can be divided into two main categories: static power and dynamic power.

Static power is the power dissipated by a gate when it is inactive, i.e. when it is not switching. The components of static power dissipation have a minor contribution to the total power dissipation, and can be minimized for well-designed circuits. Dynamic power dissipation is the dominant source of power dissipation in CMOS circuits, occurs while the circuit is switching. Charging/discharging of the load capacitances of transistors is the main source of dynamic power dissipation [8]. The energy consumed from the source for charging the output from 0 to 1 is given by equation

$$P = V^2 C_i f$$

Where C_i is the load capacitance. Only half of this energy is stored in the capacitor, while the other half is converted into heat. Similarly, when the output switches from 1 to 0 the capacitor discharges through the pull down network and the same amount of energy is dissipated as a heat. The rate at which the outputs change their value determines the average dynamic power dissipation. This is mainly dependant on the circuit activity, which can be particularly problematic during test.

Many techniques have been introduced to minimise the power consumption of new VLSI systems as the design for low power has become one of the greatest challenges in high performance VLSI design. Most of these methods focus on the power consumption during normal mode operation (functional operation), while test mode operation has not normally been a predominant concern. However, it has been found that the power consumed during test mode operation is often much higher than normal mode operation because of the high switching activity in the nodes of the CUT during test. In [1] it has been shown that the power consumed in test mode can be more than twice the power consumed in normal mode. The main reasons for this increase in test power [2, 3] are as follows:

- Modern ATPG tools generate test patterns with a high toggle rate in order to reduce pattern count which leads to a shorter test application time. Thus increasing the switching activity of CUT in test mode.
- In test mode parallel testing is often used to reduce test application time, this parallelism inevitably increases power dissipation during testing.

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- The DFT circuitry inserted in the circuit will mostly be idle during normal mode but may be used intensively during test mode, hence increasing the power consumption.
- The test vectors generated by a TPG such as LFSR, there is no definite correlation; this will increase the switching activity in the circuit.

The excessive switching activity causes many problems such that the circuit may malfunction if the temperature is too high or it can be permanently damaged as a resulting in an excessive heat dissipation, low power testing has become a very important issue to be considered in order to avoid reliability problems and manufacturing yield loss due to high power dissipation during test in VLSI circuits. Modern design and package technologies make external testing more and more difficult, and built-in self test (BIST) has emerged as a promising solution to the VLSI testing problem.

[2] MSIC-TPGs

To test the circuit, generally Automatic Test Equipment (ATE) tool is used, as it is too expensive, Built in Self Test (BIST) process was introduced. It is a DFT technique which makes the electrical testing of a chip easier, faster, more efficient, and less costly. **Logic built-in self-test** (or **LBIST**) is form of built-in self-test (BIST) in which hardware and/or software is built into integrated circuits allowing them to test their own operation, as opposed to reliance on external ATE. A typical BIST architecture consists of a test pattern generator (TPG), usually implemented as a linear feedback shift register (LFSR), a test response analyzer (TRA), implemented as a multiple input shift register (MISR), and a BIST control unit (BCU), all implemented on the chip. Depending on the Test patterns applied to the CUT. The BIST is classified into 2schemes as:

i) TPC (Test-per-clock) ii) TPS (Test-per-scan)

In TPC scheme for every clock period a new test pattern generated by the LFSR will be applied to the input of the CUT .The advantage of this scheme is that it has a shortest fault simulation time but hard to implement.Where as in TPS scheme for every $m+1$ clock cycles, where m is the number of flip-flops in a scan chain, the test patterns generated will be loaded into the scan chains applied to the CUT is captured into the scan chain and scanned out during next m scan cycles and loaded into a response analyzer; the next test pattern is scanned in concurrently. The advantage of *test-per-scan* scheme is related to the hardware savings in the MISR. Abu Issa et al., [4] proposed a new design for scan based BIST application called Bit Swapping LFSR (BSLFSR) which reduces the number of transitions that occur at the scan chain input during scan shift operation thereby dynamic power is substantially reduced. Seongmoon wang et al.,[5] proposed a new method which reduces both average power consumption and switching activity by means of operating two LFSRS at different speeds Dual Speed LFSR (DS-LFSR).LIANG *et al*.: [6] proposed a new design for Test Pattern generation [TPG] for BIST scheme applications called MSIC-TPG i.e. Multiple Single Input Change Vectors which reduces the number of transitions occurred when the test patterns applied to the CUT, thus the dynamic power dissipation is substantially reduced. This design consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block. This design develops a TPG scheme that converts an SIC vector to unique low transition vectors for the multiple scan chains. Depending on the scan length the SIC generator generates the Johnson codeword and Johnson vector using the reconfigurable Johnson counter and scalable SIC counter. A reconfigurable Johnson counter is preferred to generate an SIC sequence for shorter scan length, as shown in the figure1 which mainly operates in 3modes: Initialization mode, Circular shift register mode, normal mode.

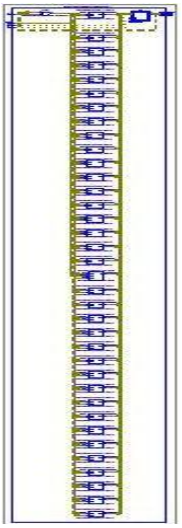

Figure 1 Reconfigurable Johnson Counter

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A SIC counter also called as Scalable SIC counter is developed for maximum scan length *l* is much larger than the scan chain number M. This MSIC-TPG is used for Test-per-clock and Test-per-scan schemes. In these schemes a conventional LFSR (Linear Feedback Shift Register) is used for the seed generator to generate the seed, which get Xored with the output of the Johnson counter value and then applied to the input of the CUT. In this method the number of transitions between the vectors generated by the TPG is very low, which substantially reduces the dynamic power dissipation.

[3] PROPOSED METHOD

The proposed new technique uses a modified LFSR to generate a random pattern and then implement a wrapper circuit and modify the controller to generate a pattern with a lower number of bit changes per pattern. This will effectively reduce the power consumption during testing. The circuit will be verified on CUT i.e. c432 bench mark circuit. The patterns generated by the modified LFSR are the low power patterns which reduce the switching activity between the two successive test patterns, by increasing the correlation between them. This proposed architecture will generate three intermediate patterns between every two successive test patterns, such that the number of switching activities between and these two and the total number of switching activities between all five patterns will be the same, an R-injector circuit will be used to generate those intermediate patterns. In this technique a 36 bit LFSR, an R-injector circuit are designed; a multiplexer is used to select the output from the shift register and the R-injector output, which is then applied to the C432 bench mark circuit. The output of the CUT is given to the Multiple Input Signature Analyzer (MISR). The signature came from the MISR will be compared with the actual signature which is already stored in the Test Response Analyzer (TRA).The modified LFSR when compared with the conventional LFSR consist of an additional circuitry as shown in the figure 2.

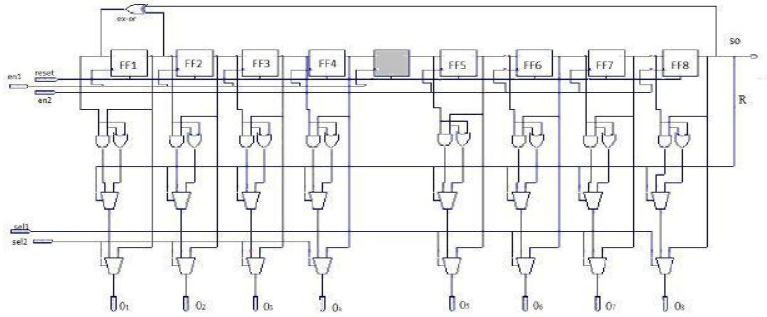

Figure 2 RTL Schematic of Modified LFSR [7]

The M_TPG is activated by two non-overlapping enable signals (en1 and en2). Each enable signal activates one half of the LFSR. In other words, when en1en2=10, first half of the LFSR is active and the second half is in idle mode. The second half is active when en1en2=01. The shaded flip flop between n/2th and n/2 +1th flip flops is used to store the n/2th bit of the LFSR when en1en2=10 and that bit is used for the second half when en1en2=01. MUX selects either the injection bit or the exact bit in the LFSR. One small finite state machine (FSM) controls the pattern generation process as follows:

Step 1: en1en2=10, and sel1sel2=11. The first half of the LFSR is active and the second half is in idle mode. Selecting sel1sel2=11, both halves of the LFSR are sent to the outputs (O1 to On). In this case, T i is generated.

Step 2: en1en2=00, and sel1sel2=10. Both halves of the LFSR are in idle mode. The first half of the LFSR is sent to the outputs (O1 to On/2), but the injector circuit outputs are sent to the outputs (On/ 2 +1 to On), Tk1 is generated.

Step 3: en1en2=01, and sel1sel2=11. The second half of the LFSR is active and the first half of the LFSR is in idle mode. Both the halves are transferred to the outputs (O1 to On), Tk2 is generated.

Step 4: en1en2=00, and sel1sel2=01. Both the halves of the LFSR are in idle mode. From the first half the injector outputs are sent to the outputs of M_TPG (O1 to On_2) and the second half sends the exact bits in the LFSR to the outputs (On/2 +1 to On) ,Tk3 is generated .

Step 5: The process will continues by going through the Step 1 to generate T i+1.

The LP-TPG with R-injection keeps the random nature of the test patterns intact. The FSM controls the test pattern generation through steps 1 to 4 and it is independent of the LFSR size and polynomial. Clk and test en are the inputs of the FSM. When test en=1, FSM starts with step 1 by setting en1en2=10 and sel1sel2=11.and it continues the process by going through step 1 to step 4. One pattern is generated for every clock cycle.

RI method inserts a new intermediate pattern between two consecutive test patterns by positioning a random-bit (R) in the corresponding bit of the intermediate pattern when there is a transition between corresponding bits of pattern pairs. Circuit is as shown in the figure 3, where the output of the R-injector circuit depends on the value of the selection line of the multiplexer "SEL".The value at the last flip flop of the shift register is given as an

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SEL input. When "SEL=0", the output of AND gate is observed at the output of the R-injector circuit, otherwise OR gate output is given as a R-injector circuit output.

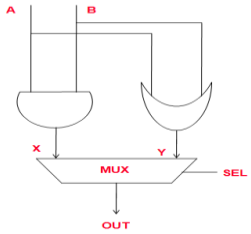

Figure 3 R-injector circuit [7]

The test vector from the proposed method has the favourable properties such as uniqueness of the test vectors, increased correlation among the test vectors. Now, this modified LFSR is used for MSIC_TPG of Test-per clock and Test-per-scan schemes as a seed generator for generating the test patterns whose schematics are shown in the figure 4&5, which are then applied to the input of the C432 bench mark circuit.

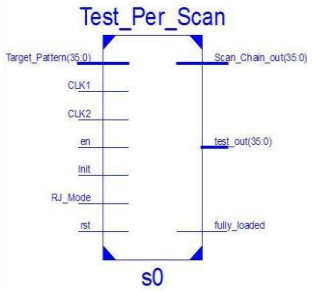

Figure 4 RTL Schematic of TPS scheme.

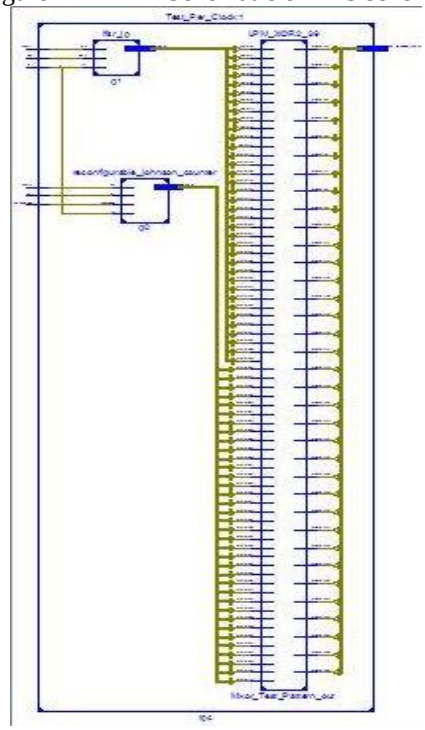

Figure 5 RTL Schematic of TPC with Modified LFSR

[4] c432 BENCHMARK CIRCUIT

ISCAS -85 c432 is a 27-channel interrupt controller. It consists of total 160 gates: 36 inputs; 7 outputs. The input channels are grouped into three 9-bit buses (we call them A, B and C), where the bit position within each bus determines the interrupt request priority. A fourth 9-bit input bus (called E) enables and disables interrupt requests within the respective bit positions. The architecture of the circuit consist of Modules labeled M1, M2, M3, M4 contain the underlying logic. The seven outputs PA, PB, PC and Chan [3:0] specify which channels have acknowledged interrupt requests whose schematic is shown in the figure 6.

The two test pattern generators: conventional TPG and LP-TPG are applied to inputs of c432 (CUT) to estimate dynamic power consumption and the area for Test-per-clock and Test-per-scan. The results are shown in table I.

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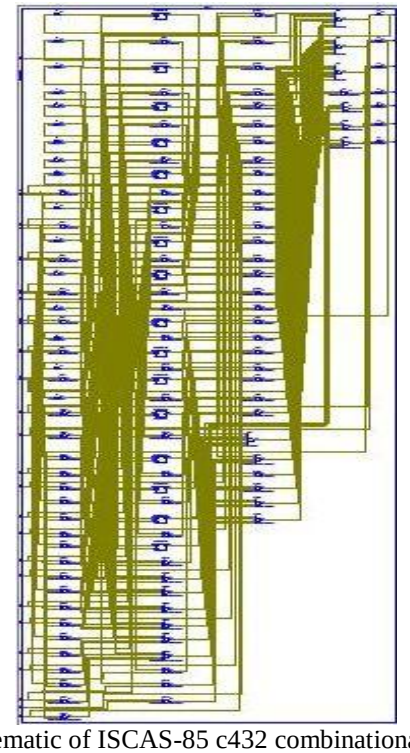

Figure 6 RTL Schematic of ISCAS-85 c432 combinational benchmark circuit

[5] EXPERIMENTAL RESULTS

To analyze the switching activity and dynamic power consumption of proposed method, the patterns generated by the both techniques are applied as input stimulus to ISCAS 89 c432 benchmark circuit for Test-per-clock and Test-per-scan schemes. The simulations are carried out in using Modelsim simulator by Verilog HDL. The power calculation will be done using Xilinx xpower tool by implementing the design simulation in Spartan3E FPGA Xilinx environment. The simulation results for Test-per-clock and Test-per-scan scheme replacing conventional TPG by Modified TPG in modelsim is shown in the figure 7 & 8.

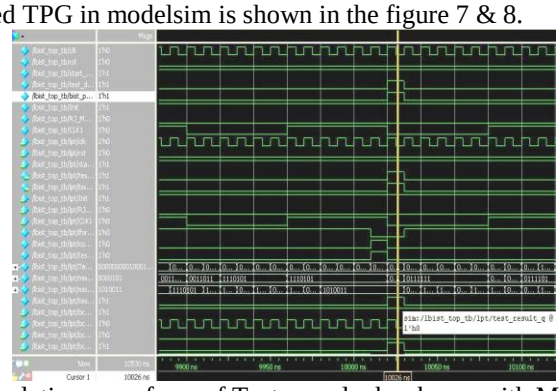

Figure 7 Simulation waveform of Test-per-clock scheme with Modified TPG.

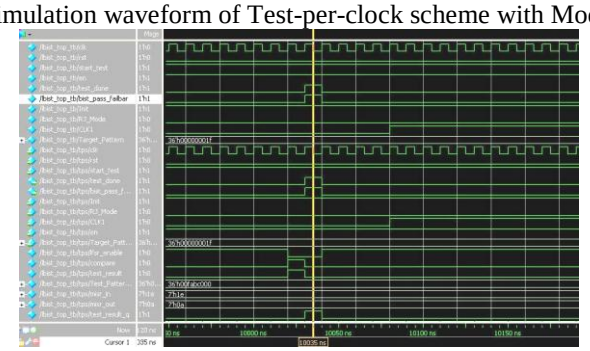

Figure 8 Simulation waveform of Test-per-scan scheme with Modified TPG.

The output of the Modified TPG is applied to the c432 combinational benchmark circuit for both the schemes and its numerical result of TPS and TPC schemes using M_TPG is 12% and 21% reductions of dynamic power consumption are analysed by the below graphical analysis and summarised in Table I.

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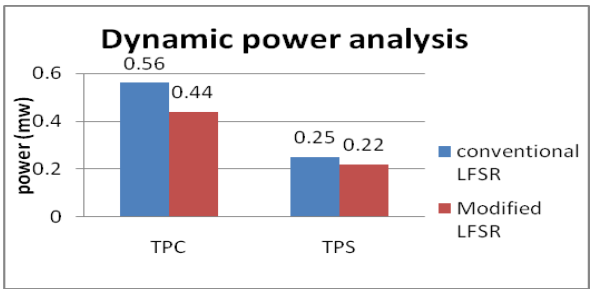

Figure 9 Dynamic power analyses

Table I. Performance Comparison

Parameter	Conventional LFSR		Modified LFSR	
	TPC	TPS	TPC	TPS
POWER (mW)	0.56	0.25	0.44	0.22
AREA(no of slices,LUTs,IOBs used)	507	4666	636	4578
Path Delay (n sec)	6.179	6.083	6.083	6.083

[6] CONCLUSION

The proposed technique generates a low power PRPG is implemented and applied on an industry standard c432 combinational benchmark circuit for dynamic power consumption estimation. The comparison of dynamic power consumption by the circuit demonstrates 12% and 21% lower power consumed by the circuit when using low power pattern as the input stimulus compared with the input stimulus generated by the conventional LFSR based MSIC-TPG schemes. The new low-power LFSR to reduce the dynamic power of a circuit during the test mode, by increasing the correlation between the test pattern, the switching activity in the circuit under test and eventually the power Consumption is reduced. The experimental results indicate up to 12% and 21% reduction in dynamic power, respectively. From table I the proposed method saves not more than the 1.86% of the area overhead for TPS scheme. It also reduces the output required time for TPC scheme and for TPS scheme it remains same.

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