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LOW-POWER DUAL-EDGE TRIGGERED CROSS-COUPLED SENSE -AMPLIFIER FLIP-FLOP

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ABSTRACT
As the power budget of today's portable digital circuit is severely limited, it is important to reduce the power dissipation in clock distribution network and flip-flops. Dual-edge triggering sense-amplifier flip-flop (DET-SAFF) is suitable for low power and high speed applications. To further reduce the power consumption at low input switching activities the "cross coupled sense amplifier flip-flop (CC-SAFF)" circuit is engaged. CC-SAFF exhibits both the low power and high speed properties, with delay and power reduction up to 44.50% and 62.94%compared to the DET-SAFF.
Keywords: sense amplifier flip-flop, clock-gated, cross coupled sense amplifier flip-flop (CC-SAFF).

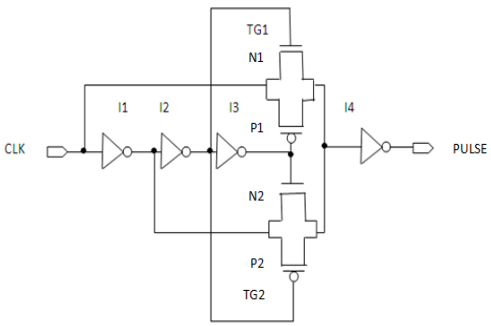
[1] INTRODUCTION

The increasing trend of portable hand held electronic devices have set a goal of high performance computing with lower energy consumption. The focus of VLSI designer is to achieve best possible trade off between power and delay for a circuit while keeping smallest possible area and complexity to reduce the overall cost of manufacturing. High performances flip-flops are key elements in the design of contemporary high-speed integrate circuits. As the power budget of today's portable digital circuit is severely limited and it is important to reduce the power distribution in both clock distribution networks and flip-flops.
Dual edge triggering is a technique to reduce the power consumption. Dual edge triggered flip-flop (DET-FF) is capable of capturing data on both rising and falling edge of the clock. The main advantage of (DET-FF) is their operation at half the frequency of the conventional single-edge clocking while obtaining the same data throughput, ref [2]. The operation of existing flip-flop architectures; analyzed their weakness, that it has some delay. So, to avoid the delay the new dual edge triggered sense-amplifier based flip-flop (DET-SAFF) circuits are proposed ref [8].

[2] TECHNIQUES FOR IMPLEMENTING DUAL EDGE TRIGGERED FLIP-FLOPS

2.1 Static-output controlled discharge flip-flop (SCDFF)

Static-output controlled discharge flip-flop consists of two stages: the pulse generator and the static latch stage ref [5]. The figure 2.1(a) and 2.1(b) shows the pulse generator and the latch. The latch that captures the pulse signal and the input D is used to drive the pre-charge transistor so that node X follows D during the sampling period. The conditional discharging technique is implemented by inserting a QB-controlled NMOS in the discharge path, which presents unnecessary discharging at node X as long as the input remains high.



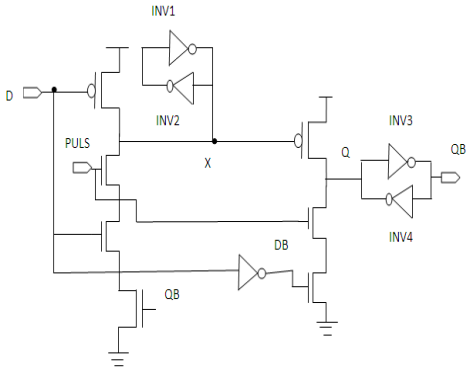


Fig 2.1(a) Pulse generator Fig 2.1(b) Static latch

The advantage of static output–controlled discharge flip-flop (SCDFF) is low power consumption, but the drawback is delay.

2.2 Dual edge triggered static-pulsed flip-flop (DSPFF)

The dual edge triggered static-pulsed flip-flop (DSPFF) consists of pulse generator is shown in figure 2.2(a) and static latch is shown in figure 2.2(b). The pulse generator design incorporates four inverters which one used to generate the inverted and delayed clock signals. These signals along with two NMOS transistors generate a

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narrow sampling window at both the transition edges; rising and falling edges. In static latch; the pulse signal is generated by the pulse generator circuit; both NMOS pass transistors N1 and N2 are

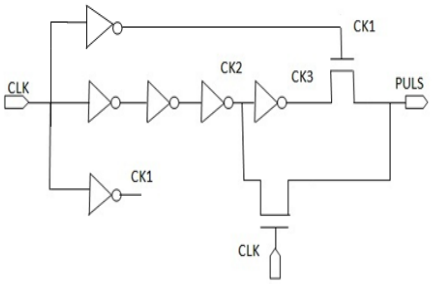

Fig 2.1 (a) pulse generator

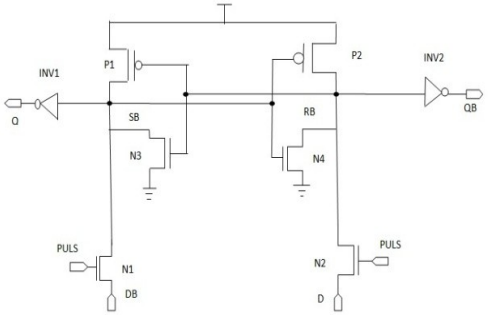

Fig2.2 (b) static latch

Switched on to pass the input data, so that either SB or RB will be discharged. The PMOS transistors, P1 and P2 together with two weak NMOS transistors N3 and N4 effectively avoid the floating of nodes SB and RB when the flip-flop is opaque ref [6]. The feature of dual edge triggered static pulsed flip-flop (DSPFF) eliminates unnecessary transition. It suffers from high leakage current; this caused by a high- voltage drop across either transistor N3 or N4; when they are off.

2.3 Adaptive clocking dual edge triggered sense amplifier flip-flop (ACSAFF)

The adaptive clocking dual edge triggered sense amplifier flip-flop (ACSAFF) is shown in figure 2.3.It consists of three stages: adaptive clocking inverting stage, sensing stage and the NIKOLIC'S latch stage. Recently reported flip-flop structures achieved a small delay between the latest point of arrival and output transitions. So typical representative of these structures are sense amplifier–based flip-flop (SAFF).The adaptive clock inverter chain is designed to disable some internal clocked transistors when the data switching activity is low ref [7]. The adaptive clocking inverter chain is as shown in below figure 2.3(a)

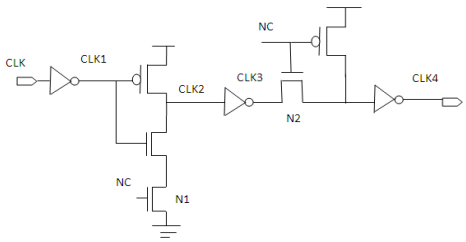

Fig 2.3(a) Adaptive clocking inverter chain

In the sensing stages; if input D is different from output Q, node NC is pulled up, to turn on transistors N1and N2. Consequently, the desired inverted and delayed signals, CLK3 and CLK4 will be produced so that a narrow sampling transparent window is created on the rising or the falling edges of the clock, either SB or RB will be discharged during the transparent period. So it changes the output state. Once the output state is altered the charging path of NC is blocked and NC will be discharged through the N3and N4 or N5 and N6, thereby disabling the inverter chain .When D is same as the Q, then the node NC will be low and the flip-flop is opaque. NIKOLIC'S latch is a type of latch to improve the speed of the circuit ref [10]. Let us examine with more details the operation and the performance of the latch. If SB and RB are high, then the latch in the hold state .In fact, S and R are both low then the devices are N1, N2, P1, and P2 are off. The devices N3, N4, P4, and P6 hold the latch state. If SB low; device P1is is turned ON, and the node Q is quickly driven high. Since N1 is off and SB also shuts off devices N3 which opens the remaining pull-down path for Q node. Moreover the signal goes high, and the transistor N2 turns on driving the QB is low.

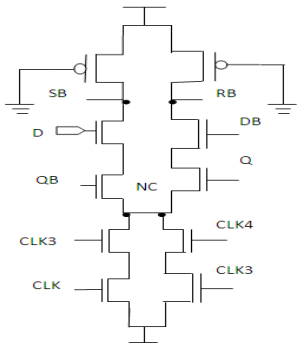

Fig 2.3(b) sensing stage

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The adaptive clocking dual edge triggered sense-amplifier flip-flop (ACSAFF) requires more transistors and hence causing the circuit to be more complex. This will lead to great power consumption at high switching activity and the degradation of the flip-flop speed.

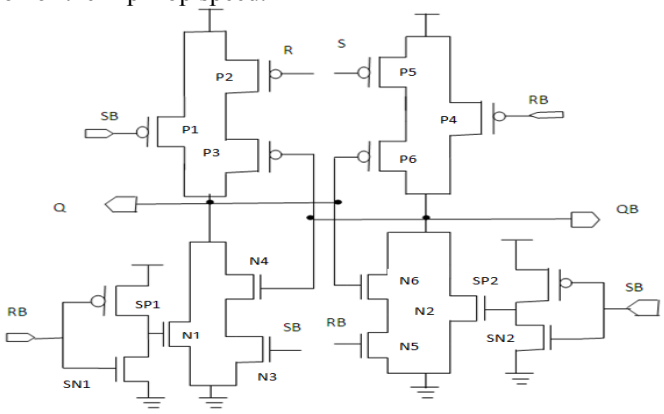

Fig 2.3(c) NIKOLIC'S latch

2.4 Dual edge triggered sense-amplifier flip-flops

The two new dual edge triggered sense-amplifier flip-flops are proposed in this section. One is dual edge triggered sense amplifier flip-flop (DET-SAFF) and the other one is the clock gating sense amplifier flip-flop (CG-SAFF).

2.4.1 Dual edge triggered sense- amplifier flip-flop (DET-SAFF)

The dual edge triggered sense amplifier flip-flop mainly consists of three stages. The pulse generating stage, sensing stage and the latching stage. In DET-SAFF the simple pulse generator is used as ref [9], it can be shown in figure 2.4.1(a). The pulse generator produces a brief signal at rising and falling clock edges. The sensing and the latching stages of the dual edge triggered sense-amplifier flip-flop are shown in figure 2.4.1(b) and figure 2.4.1(c). In the sense amplifier stage, the input D is low, SB will be set to high, and if D is high, RB will be set to high. To avoid the redundant transitions in the internal nodes the conditional pre-charging technique is used.

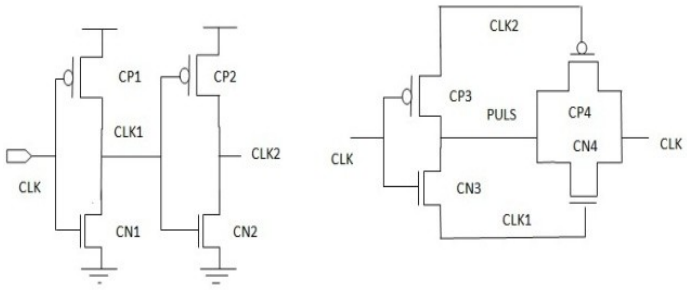

Fig 2.4.1(a): pulse generator

In this dual edge triggered sense amplifier flip-flop a fast symmetric latch is developed, it can be shown in figure 2.4.1(c). To improve the operating speed and it is similar to the NIKOLIC'S latch and STROLLO'S latch ref [10]. The symmetric latch uses SB and RB to pull up the output nodes, the pull down path is modified as with a PULS-controlled NMOS pass transistor, through which D is directly connected to the Q and DB which is directly connected to the QB node

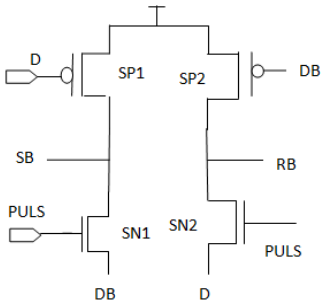

Fig 2.4.1(b) sensing stage

This increases the speed of the high to low transition, because the output latch immediately captures the input value once the PULS signal is generated. And it also improves the low to high latency because the output node will be charged by the pull-up (LP1 and LP2) transistors and also by the pass (LN1 and LN2) transistors. The pass transistors cannot fully charge a node to high but helps for pull-up transition, and the other

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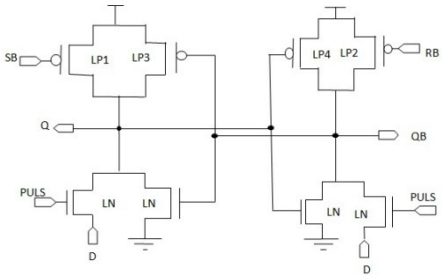

Fig 2.4.1(c) symmetric latch

four inner transistors LP3, LP4, LN3 and LN4 are used for the purpose of maintaining output state, when the flip-flop is opaque. The dual edge triggered sense-amplifier flip-flop is a technique to the power saving, and it is applicable to the latch part of the flip-flops, when the switching activity of the clock is 1, the pulse generator always be operating even when the output has no changes. Due to this, the unnecessary transitions causes a lot of power is wasted, and it consumes a high power at low input switching activities.

2.4.2 Clock gated sense-amplifier flip-flop (CG-SAFF)

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. The clock gated sense amplifier flip-flop (CG-SAFF) is constructed to eliminate the unnecessary transitions in the pulse generator. In this, the DET-SAFF design is used as a baseline circuit and the clock gating technique is incorporated. The CG-SAFF mainly consists of three stages: pulse generator, sensing stage and latching stage. Clock gated sense-amplifier flip-flop pulse generator stage can be shown in figure 2.4.2(a).

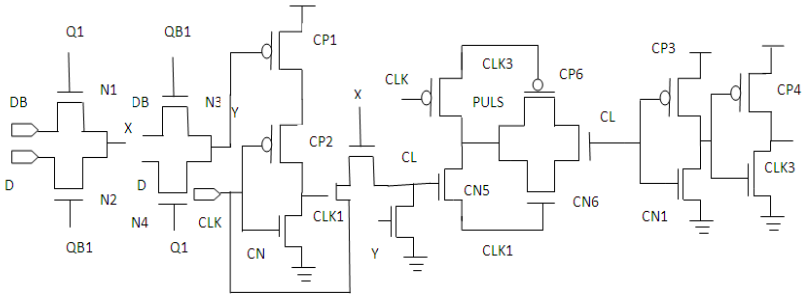

Fig 2.4.2(a): clock gated sense amplifier flip-flop pulse generating stage

In clock gated sense amplifier flip-flop pulse generating stag , to compare the previous and current input values two comparators are used to produce the signals X and Y, by making use of the inputs D and DB and the outputs Q1 and QB1. If D is different from the output Q1 then X will be pulled up to high and Y to be low. The clock signal will pass through as CL since the transistor CN3 is turned on, the clock signal CL is called as a gated clock. At the same time CP1 is turn on and drive the signal CLK1to high before the rising edge of the clock. The clock signal CL is high and its delayed signal CL3 remains low at rising edge of the clock., then the transistor CN5 to ON to drive the PULS signal to high, when the CLK1 is low and the CLK3 is pulled up the transparent window is closed as after a short period time. Hence at the rising edge of the clock a short transparent period is introduced.

The signal CLK1 is used for the pulse generation rather than CLK2, so that the flip-flop only captures the data at the triggering edge of the clock. At the falling edge of the clock CL is low and the CLK3 is high. The transistor CP5 is selected and it generates a high PULS signal, when the clock is low the sampling window is shutdown. When the signal s X will be low and the Y will be high, when the input D remains at consecutive clock cycles, CLK3 will be low without considering the CLK signal only if the CL is pulled down by CN4. CLK1 is discharged at the first clock cycle and maintain its low state in the remaining clock cycles, thus makes the flip-flop is opaque and thus the power can be saved.

Clock-gated sense amplifier flip-flop (CG-SAFF) sensing stage is shown in figure 2.4.2 (b).The sensing stage of the clock-gated sense amplifier flip-flop is same as sensing stage of DET-SAFF.

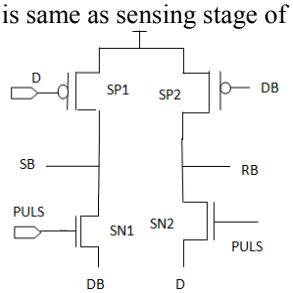

Fig 2.4.2(b) Sensing stage

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Clock-gated sense amplifier flip-flop (CG-SAFF) latching stage is shown in figure 2.4.2(c) The PULS signal of the CG-SAFF is heavily loaded comparing with DET-SAFF, a different latch is used in the in CG-SAFF, it does not require any clock signal and provides the most stable operation. To obtain the differential outputs Q1 and QB1 with reduced the load capacitances the inner holding topology is modified. The clocking stage Q1 and QB1 are used to generate the X and Y instead of using Q and QB.

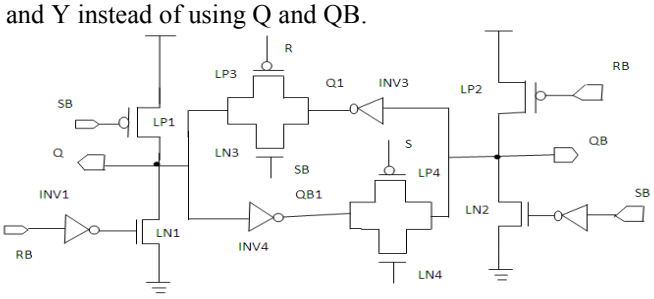

Fig 2.4.2(c) latching stage

[3] MODIFIED METHOD

3.1 Cross coupled sense amplifier flip-flop

In order to reduce the power further, the clock gating sense amplifier flip-flop latching stage is modified with cross coupled sense amplifier flip- flop. Cross coupled sense amplifier flip-flop mainly consists of three stages. Clock gated pulse generator, sensing stage and the latching stage.

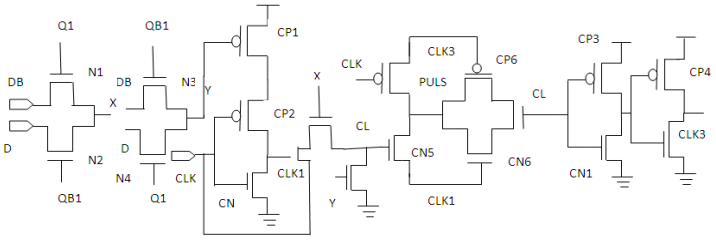

Fig 3.1(a) clock gated pulse generator

In this technique the clock pulse generator and the sensing stage is shown in fig 3.1(a) and 3.1(b). This is same as CG-SAFF.

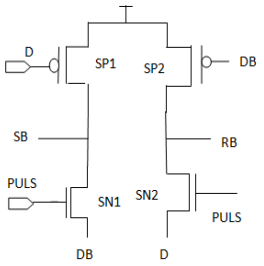

Fig 3.1(b) sensing stage

The latching stage of the cross coupled sense amplifier flip-flop is shown in below figure 3.1(c). The clock gated sense amplifier flip-flop latching stage is modified with cross sense amplifier flip-flop that is based on the two cross coupled CMOS inverters.

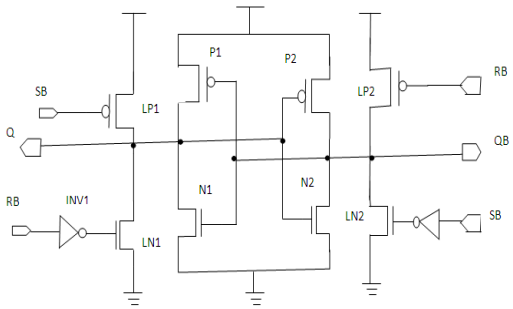

Fig3.1(c) latching stage

When SB is low the pull up transistor LP1 transistor conducts to high, then Q is immediately drives to high and charged to VDD and LN2 pull down transistor is on; discharged to ground. RB is high and the inverter I1 becomes low, then the pull down transistor LN1 is off. And the LP2 pull up transistor off, then QB is low. The P1, N1, P2 and P2 transistors are used to maintain the output state when the flip-flop is opaque.

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[4] SIMULATION RESULTS

The simulated wave form of modified CC-SAFF can be shown in below figure 4.1.

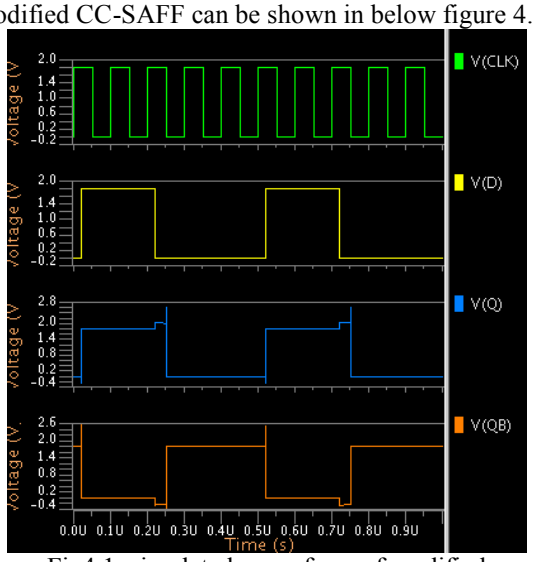

Fig4.1: simulated wave form of modified CC-SAFF

To evaluate the performance of the modified flip-flop, comparisons had been performed with other dual edge-triggered designs, SCDFF, DSPFF, ACSAFF, DETSAFF, CGSAFF, and CCSAFF. All the flip-flops were designed using chartered semi conductor limited's 0.18µm CMOS process technology, at an operating temperature of 27c and a supply voltage of 1.8v, using mentor graphics. The power, delay, rise time, fall time, results for various simulation stages are tabulated in below table1. And the power delay product performance comparison at low input switching activities can be shown in table2.At 1v input switching activity CC-SAFF offers 94.3% power reduction and delay 38.07% compared to the CGSAFF. At 0.67v input switching activity CC-SAFF offers 95.18% power reduction and delay 86% compared to the CGSAFF and at 0.5v input switching activity CC-SAFF offers59.78 % power reduction and delay30.24 % compared to the CGSAFF. Figure 4.2 and figure 4.3 presents the delay and power comparison results for different techniques. The modified technique CC-SAFF exhibits its superiority in power saving by 62% and reduced delay by 44%.

Table1: performance comparison

FLIP-FLOPS	Rise time(ps)	Fall time(ps)	Delay (ps)	Avg power(uw)	PDP(fj)
SCDFF	374.2	259.3	307.1	229.5	70.4
DSPFF	310.5	223.2	270.9	586.1	158
ACSAFF	098.5	081.6	012.3	3435	42.2
DETSAFF	135.4	171.6	199.5	772.4	154
CG-SAFF	170.4	176.5	160.7	452.2	72.6
CC-SAFF	071.3	024.2	089.3	167.5	14.9

Table 2: Power delay product (PDP) performance comparison at low input switching activities.

DESIGNS	CG-SAFF	CC-SAFF
PDP(1V)	19.4	6.7
PDP(0.67V)	0.68	0.23
PDP(0.5V)	0.63	0.17

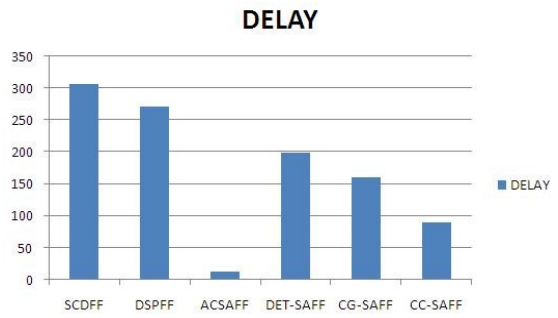

Figure 4.2: Delay performance

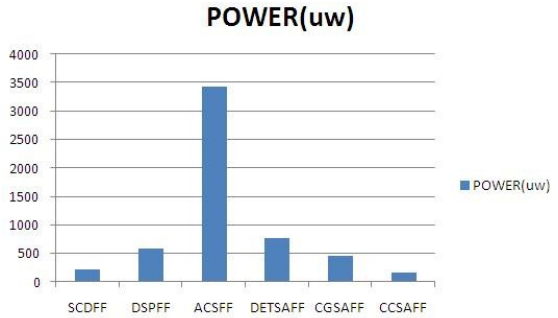

Figure 4.3: power performance

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CONCLUSION

A dual edge triggered sense amplifier flip flop for low power and high performance applications is presented in this paper. By incorporating conditional pre-charging and DET-SAFF is obtained with power reduction. CG-SAFF is superior in power saving at low switching activities; further a modified version of CG-SAFF is introduced by incorporating CC-SAFF, which significantly improves the power and delay parameters by62% and 44%. CC-SAFF is superior in power delay product savings at low input switching activities.

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