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# REALISATION OF VEDIC MULTIPLIER USING URDHVA TIRYAKBHAYAM SUTRA

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**ABSTRACT**

*Multiplication is the one of the basic arithmetic operations and it requires and more processing time and power than other arithmetic operations like addition and subtraction. So, multiplier design is always a challenging task, however many designs are proposed, the user needs demands much more optimized ones. Vedic mathematics provides some algorithms that evaluate fast results, both in mental calculations or hardware design. Power dissipation is continuously reduced by the use of Reversible logic. The reversible Urdhva Tiryakbhayam Vedic multiplier is one such multiplier which is effective both in terms of speed and power. In this paper the modified design increase the performance by maintain the design functionality without any degradation. The Total Reversible Logic Implementation Cost (TRLIC) evaluate the proposed design. This multiplier has application over designing Fast Fourier Transforms (FFTs) Filters and other applications of DSP like imaging, software defined radios, wireless communications.*

***Keywords:*** *REVERSIBLE GATES, Urdhva Tiryakbhayam , Vedic mathematics.*

## [1] INTRODUCTION

High speed arithmetic operations are very important in many signal processing applications. Speed of the DSP (digital signal processing) processor is largely determined by the speed of its multipliers. In fact the multipliers are the most important part of all DSP processors in realizing many important functions such as fast Fourier transforms and convolutions. Multiplication can be implemented using many algorithms such as array, booth, carry save, and Wallace tree algorithm. The computational time required by the array multiplier is less because the partial products are computed independently in parallel. The delay associated with the array multiplier is the time taken by the signals to propagate through the gates that form the multiplication array.

Arrangement of adders is another way of improving multiplication speed. There are two methods for this: Carry save array (CSA) method and Wallace tree method. In the CSA method, bits are processed one by one to supply a carry signal to an adder located at a one bit higher position. The CSA method has a limitation in the delay performance. In the Wallace tree method, due to complexity of circuit, the circuit lay out is not easy.

Booth algorithm reduces the number of partial products. However, large booth arrays are required for high speed multiplication and exponential operations which in turn require large partial sum and partial carry registers. Thus, a large propagation delay is associated with this case. The modified booth encoded Wallace tree multiplier uses modified booth algorithm to reduce the partial products and also faster additions are performed using the Wallace tree**.**

As more transistors per chip became available due to larger-scale integration, it became possible to put enough adders on a single chip to sum all the partial products at once, rather than reuse a single adder to handle each partial product one at a time. Because some common DSP algorithms spend most of their time multiplying, DSP processor designers sacrifice a lot of chip area in order to make the multiply as fast as possible; a single-cycle multiply–accumulate unit often used up most of the chip area of early DSPs.

## [2] VEDIC MATHEMATICS

Vedic Mathematics is one of the most ancients methodologies used by the Aryans in order to perform mathematical calculations. This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works.

Vedic mathematics can be aptly employed here to perform multiplication. Another important area which any DSP engineer has to concentrate is the power dissipation, the first one being speed. There is always a trade-off between the power dissipated and speed of operation. The reversible computation is one such field that assures zero power dissipation. Thus during the design of any reversible circuit the delay is the only criteria that has to be taken care of. In a reversible Urdhva Tiryakbhayam Multiplier had been proposed.

### 2.1. Reversible Logic Gates:

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. The fanout in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates, there are many parameters for determining the complexity and performance of circuits .

- **The number of Reversible gates (N):** The number of reversible gates used in circuit.

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- **The number of constant inputs (CI):** This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- **The number of garbage outputs (GO):** This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- **Quantum cost (QC):** This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.
- **Gate levels (GL):** This refers to the number of levels in the circuit which are required to realize the given logic functions .
- **Total Reversible Logic Implementation Cost (TRLIC) :** Let, in a reversible logic circuit there are NG reversible logic gates, CI constant inputs, GO number of garbage outputs, and have a quantum cost QC. Then the TRLIC is given as Reduction of these parameters is the bulk of the work involved in designing a reversible circuit. In this, an improved design of reversible multiplier with respect to its previous counterparts is proposed.

### 2.2. Basic reversible logic gates

- **Feynman Gate**

Figure 1 shows a 2*2 Feynman gate . Quantum cost of a Feynman gate is 1.Feynman gate is called as Controlled NOT gate or CNOT gate. It is equivalent to single control input tofili gate.

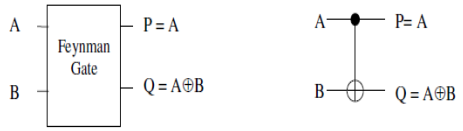


Figure 1: Feynman gate and its symbolic representation

- **Toffoli Gate**

Figure 2 shows a 3*3 Toffoli gate The input vector is I(A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=A(B xor C). Quantum cost of a Toffoli gate is 5. It has two control inputs.

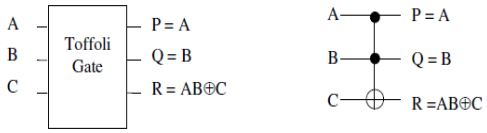


Figure 2: Toffoli gate and its symbolic representation

- **Peres Gate**

Figure 3 shows a 3*3 Peres gate [8]. The input vector is I(A,B,C) and the output vector is O(P,Q,R).The output is defined by P=A, B and Q=A B,R=AB C. Quantum cost of a Peres gate is 4.

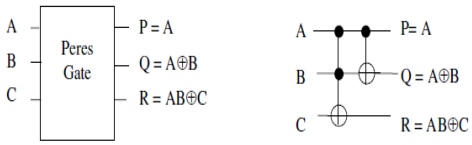


Figure 3: Peres Gate and its symbolic representation.

- **BVPPG gate:**

BVPPG gate is a 5 * 5 reversible gate and its logic diagram is as shown in figure. Its quantum cost is 10. The truth table of BVPPG is as shown in the Table -1.

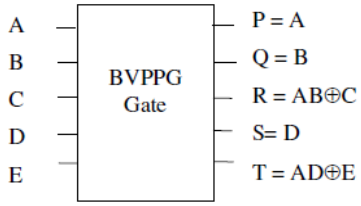


Figure 4: BVPPG Gate

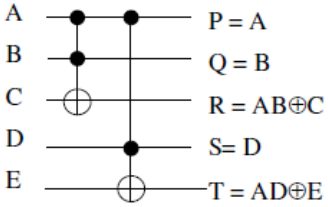


Figure 5: Toffoli Gate representation of BVPPG Gate

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The BVPPG gate is used to construct the partial product generator which has resulted in least number of gates, least quantum cost and least number of garbage outputs. The two product terms are available at the outputs R and T of the BVPPG gate with C and E inputs maintained constant at 0. The other outputs namely P, Q and S are used for fan-out of the multiplier operands as shown in figure.. This reduces the number of external fan-out gates to zero in our design which is main design feature. The proposed design is compared with the existing designs

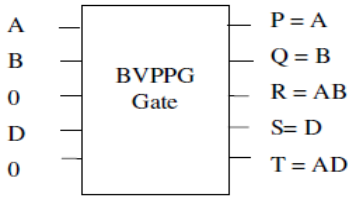


Figure 6: BVPPG Gate producing product terms and duplication of the inputs.

➢ **CNOT GATE**

CNOT gate is also known as controlled-not gate. It is a 2*2 reversible gate. The CNOT gate can be described as:

Iv = (A, B) ; Ov = (P= A, Q= A B)

Iv and Ov are input and output vectors respectively.m Quantum cost of CNOT gate is 1. Figure shows a 2*2 CNOT gate and its symbol.

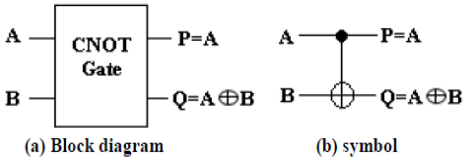


Figure 7: CNOT Gate

➢ **NFT Gate**

It is a 3x3 gate and its logic circuit and its quantum implementation is as shown in the figure. It has quantum cost five.

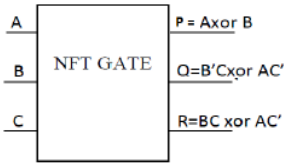


Figure 8: Block diagram of NFT Gate.

**[3] Urdhva Tiryakbhaya Multiplication Algorithm**

Urdhva Tiryakbhayam (UT) is a multiplier based on Vedic mathematical algorithms deviced by ancient Indian Vedic mathematicians. UT sutra can be applied to all cases of multiplications viz. Binary, Hex and also Decimals. It is based on the concept that generation of all partial products can be done and then concurrent addition of these partial products is performed. Unlike other multipliers with the increase in the number of bits of multiplicand and/or multiplier the time delay in computation of the product does not increase proportionately. Because of this fact the time of computation is independent of clock frequency of the processor. Hence one can limit the clock frequency to a lower value. Also, since processors using lower clock frequency dissipate lower energy, it is economical in terms of power factor to use low frequency processors employing fast algorithms like the above mentioned. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases at a slow pace as compared to other conventional multipliers.

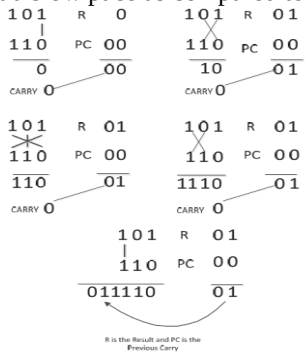


Figure 9: Urdhva Tiryakbhayam Procedure for Multiplication.

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### 3.1. OPTIMIZATION OF THE URDHVA TIRYAKBHAYAM MULTIPLIER

The conventional logic design implementation of a 2x2 Urdhva Tiryakbhayam multiplier using the irreversible logic gates is a shown in the figure. In the four expressions for the output bits are derived from this figure and is used to obtain the reversible implementation as shown in figure. The circuit uses five Peres gates and one Feynman gate. This design has a total quantum cost of 21, number of garbage outputs as 11 and number of constant inputs 4. The gate count is 6. This design does not take into consideration the fan outs. The overall performance of the UT multiplier is scaled up by optimizing each individual unit in terms of quantum cost, garbage outputs etc.

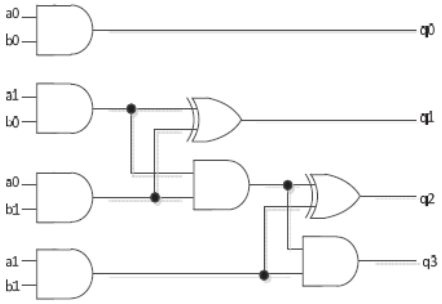


Figure 9: Conventional 2x2 Urdhva Tiryakbhayam Multiplier.

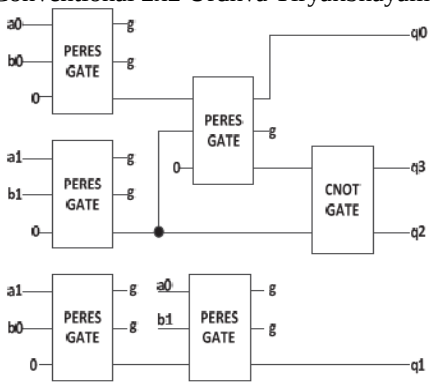


Figure 10: Reversible 2x2 UT Multiplier

### 3.2. Improved 2x2 Urdhva Tiryakbhayam multiplier

The design expressions can be logically modified so as to optimize the design. The new design makes use of one BVPPG, three Peres gates and a single Feynman gate. The design also takes into account the fan outs. One of the major design constraints of reversible logic is the fan out, other being loops not permitted. This means that the reversible logic circuit with multiple numbers of same inputs is not advisable. One way out is to use a separate fan out generator or to build a circuit that inherently takes care of fan outs using the reversible logic gates used in the design. This design has a quantum cost of 23, number of garbage outputs as 5, number of gates 5 and the number of constant inputs is 5.

The second design also considers the fan out using BVPPG, three Peres gates and one NFT gate as shown in the figure 5. The quantum cost of the circuit is 24; number of garbage outputs as 4, number of gates 5 and the number of constant inputs is 5. I1, I2, I3 (Fig 5 and 6) and I4 (Fig 6) are the intermediate outputs that are used for fan-out purposes.

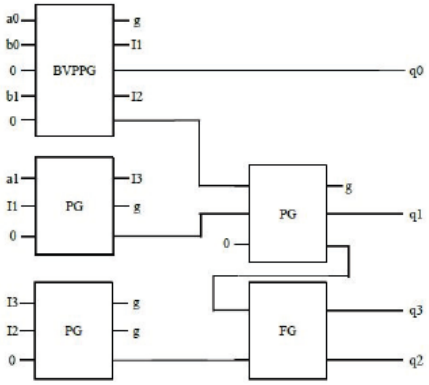


Figure 11: Proposed Modified Design 1

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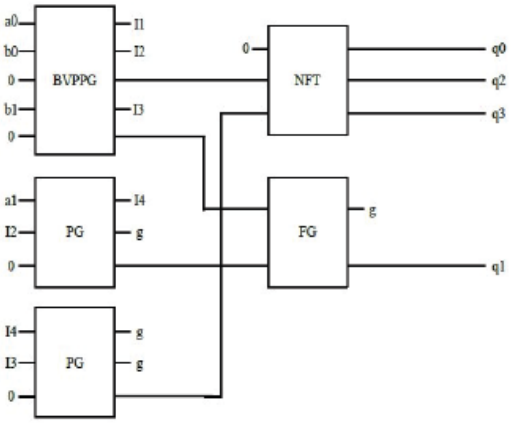


Figure 12: Proposed Modified Design 2

### 3.3. Design of 4x4 Urdhva Tiryakbhayam multiplier

The Reversible 4X4 Urdhva Tiryakbhayam Multiplier design emanates from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure 6. It consists of four 2X2 multipliers each of which procures four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication.

Two zeros are concatenated with the upper two bits and given as input to the four bit ripple carry adder. The other four input bits for the ripple carry adder are obtained from the second 2X2 multiplier. Likewise the outputs of the third and the terminal 2X2 multipliers are given as inputs to the second four bit ripple carry adder. The outputs of these four bit ripple carry adders are in turn 5 bits each which need to be summed up. This is done by a five bit ripple carry add which generates a six bit output. These six bits from the upper bits of the final result.

The design shown in consists of only HNG gates. The number of HNG gates is 4 if the ripple carry adder is used in the second stage or five if the ripple carry adder is used in the last stage of the 4X4 Urdhva Tiryakbhayam Multiplier. The ripple carry adder can be modified as under. Since for any ripple carry adder the input carry for the first full adder is zero, this implicitly means the first adder is a half adder. Thus a Peres gate can efficiently replace a HNG. This cut down the quantum cost by two for any ripple carry adder and the garbage output by one. The Constant inputs and the gate count remain unchanged.

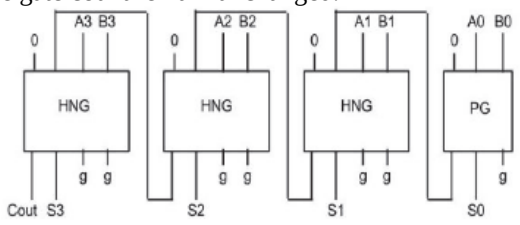


Figure 14: Proposed Modified 4 Bit Ripple Carry Adder Design.

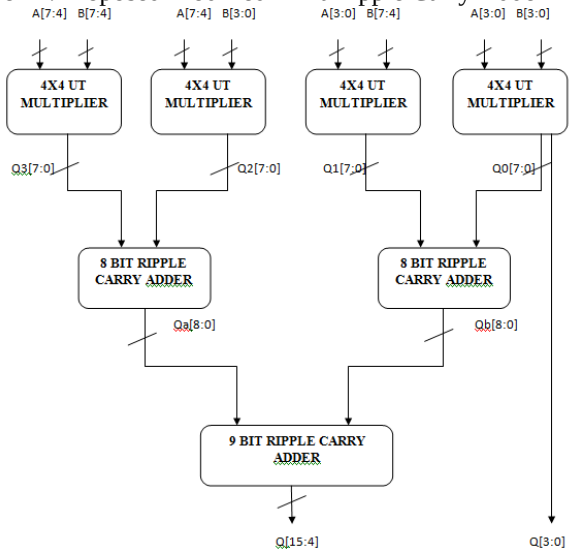


Figure 15: UT 8x8 Ripple Carry Adder Design

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Since TRLIC is the sum of all these design parameters, it is commendable of having a least value of TRLIC The proposed design of Reversible UT Multiplier is compared with as many as 11 different prominent multiplier designs in the literature in terms of Quantum cost, garbage outputs, number of gates, number of constant inputs and also in terms of TRLIC values. This also includes a comparison with our own previous design and the optimization is clearly evident from the table of comparison.

In existing design of 4x4 "Urdhva-tiryakbyham" multiplier using reversible logic gates, which are designed using2x2 "Urdhva-tiryakbyham" multiplier as a modules which is used for 2 bit multiplication which are followed by two 4 bit ripple carry adders and 1 5 bit carry adder, which is cause for increment in the delay, so in propose design the 2x2 "Urdhva-tiryakbyham" multiplier is kept as it is but instead of using 1 one 5 bit ripple carry adder ,it is replaced by 4 bit ripple carry adder, which is used for reducing the delay shown in figure 16.

Which indeed increases the performance of the design in terms of speed and reduces the power for performing the corresponding partial products. In extension to these, a 8 bit "Urdhva-tiryakbyham" multiplier is designed shown in figure17,which used a four 4 bit "Urdhva-tiryakbyham" multiplier multipliers as a modules for multiplication, which followed by two 8 bit ripple carry adders, because as the input for "Urdhva-tiryakbyham" multiplier is 4 bit ,it provides a result of 8 bit ,so these 8 bit will be given to the adders to perform additions ,but instead of using full adders in the internal block of ripple carry adders, reversible logic gates are designed so that to perform the low power operations ,as the input for 8 bit ripple carry adders is eight bits it outcomes a result of 8bit sum and one bit carry ,which is given to the 9 bit ripple carry adder, which provides the final product. An alternate approach is used with three 8 bit ripple carry adders so that, the design performs the better and fast operation, which also reduces the delay factors so by using two 8 bit ripple carry adder, and one 9 bit ripple carry adder is replaced the design with three 8 bit the delay by 7.12% and area by 8.27% is obtained.

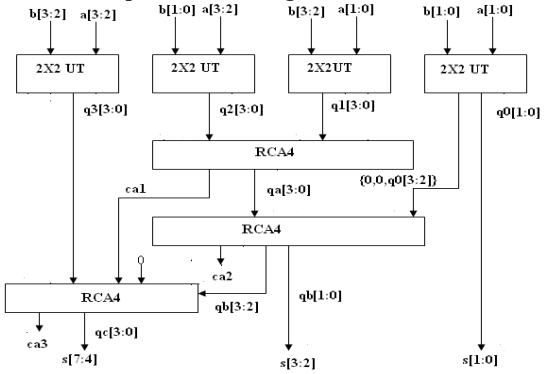


Figure 16: Proposed UT 4x4 Ripple Carry Adder

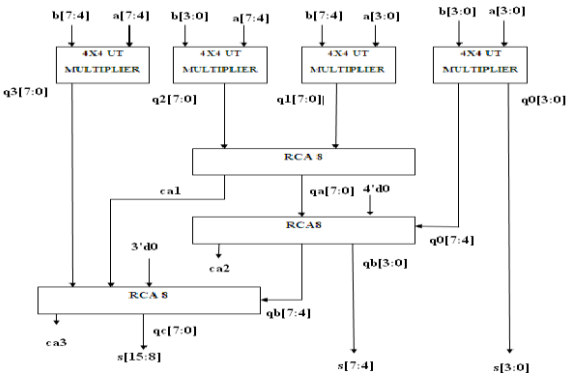


Figure 17: Proposed UT 8x8 Ripple Carry Adder

## SIMULATION RESULTS

### UT 8x8 SIMULATED WAVEFORM

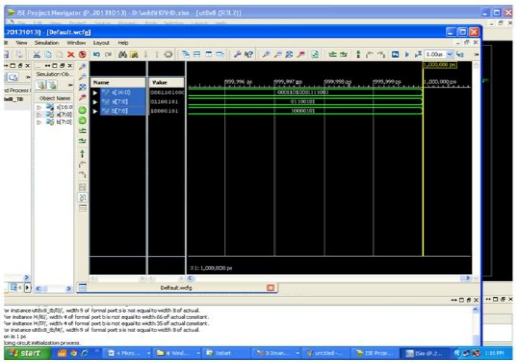

Table I: Performance Parameters

| parameters | UT 8x8 Multiplier | Proposed UT 8x8 Multiplier |
|---|---|---|
| DELAY(ns) | 30.9 | 28.7 |
| LUTs (no of fliflops, multiplier) | 145 | 133 |

The tabular form shows the parameters are optimized for the proposed design.

## CONCLUSION

Multiplication plays important role in the processors. Reversible computation is an emerging area of research, having applications in numerous fields. In this paper a reversible Vedic multiplier is proposed using Urdhva Tiryakbhyam sutra. From the table it is proved that the proposed Design an optimized area and delay of 8.27%

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and 7.12% compared with the conventional design. In this the simulation and synthesis are carried out using Xilinx-ISE tool, using target technology and performing placing & routing operation for system verification.

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