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DESIGN OF 9 BIT SAR ADC USING HIGH SPEED AND HIGH RESOLUTION OPEN LOOP CMOS COMPARATOR IN 180NM TECHNOLOGY WITH R-2R DAC TOPOLOGY

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ABSTRACT

A Successive approximation analog to digital converter (ADC) for data acquisition using fully CMOS high speed self-biased comparator circuit is discussed in this paper. ASIC finds greater demand when area and speed optimization are major concern and here the entire optimized design is done in CADENCE virtuoso EDA tool in 180nm technology. Towerjazz semiconductor foundry is the base for layout design and GDSII extraction. Comparison of different DAC architecture and the precise architecture with minimum DNL and INL are chosen for the design procedure. This paper describes the design of a fully customized 9 bit SAR ADC with input voltage ranging from 0 to 2.5V and sampling frequency 16.67 KHz. Hspice simulators is used for the simulations.

Keywords— SAR ADC, Comparator, CADENCE, CMOS, DAC.

[1] INTRODUCTION

With the development of sensors, portable devices and high speed computing systems, comparable growth is seen in the optimization of Analog to digital converters (ADC) to assist in the technology growth. All the natural signals are analog and the present digital world require the signal in digital format for storing, processing and transmitting and thereby ADC becomes an integral part of almost all electronic devices[8]. This leads to the need for power, area and speed optimized design of ADCs. There are different ADC architectures like Flash ADC, SAR ADC, sigma-delta ADC etc., with each having its own pros and cons. The designer selects the desired architecture according to the requirements[1]. Flash ADC is the fasted ADC structure where the output is obtained in a single cycle but requires a large number of resistors and comparators for the design. For an N bit[2] flash ADC 2^N resistors and 2^{N-1} comparators are required consuming large amount of area and power. Modifications are done on flash ADC to form pipelined flash ADC where the number of components can be reduced but the power consumption cannot be further reduced beyond a level. Sigma-delta ADC or integrating type of ADC is used when the resolution required is very high. This is the slowest architecture compared to other architectures. Design of sigma-delta requires analog design of integrator circuit making its design complex. SAR ADC architecture gives the output in N cycles for an N-bit ADC. SAR ADC being one of the pioneer ADC architecture is been commonly used due to its good trade-off between area, power and speed, which is the required criteria for CMOS deep submicron circuits.

SAR ADC consists of a Track and Hold (TH) circuit, comparator, DAC and a SAR register and control logic. Figure 1 shows the block diagram of a SAR ADC. This paper is organized into six sections. Section II describes the analog design of TH and comparator. Section III compares the DAC architecture. Section IV explains the SAR logic. Section V gives the simulation results and section VI is the conclusion.

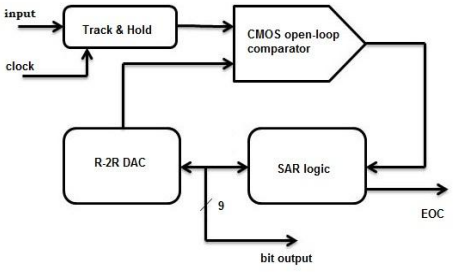

Fig 1 Block Diagram of SAR ADC

[2] ANALOG DESIGN OF TH AND COMPARATOR

A. Track and Hold

In general, Sample and hold circuit or Track and Hold contain a switch and a capacitor. In the tracking mode, when the sampling signal (strobe pulse) is high and the switch is connected, it tracks the analog input signal[3]. Then, it holds the value when the sampling signal turns to low in the hold mode. In this case, sample and hold provides a constant voltage at the input of the ADC during conversion[7]. Figure 2 shows a simple Track and hold

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circuit with a NMOS transistor as switch. The capacitance value is selected as 100pF and aspect ratio of the transistor as 28 based on the design steps.

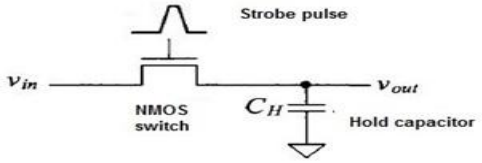

Fig 2 Track and hold circuit

B. Latched comparator

Comparator with high resolution and high speed is the desired design criteria and here dynamic latched comparator topology and self-biased open loop comparator topology are studied and implemented. From the comparison results, the best topology considering speed and better resolution is selected. Figure 3 shows a latched comparator. Static latch consumes static power which is not attractive for low power applications. A major disadvantage of latch is low resolution.

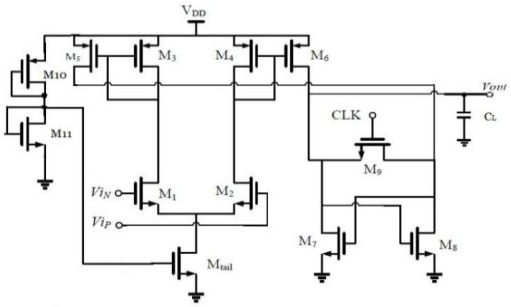

Fig 3Latched comparator

C. Self-biased open loop comparator

A self-biased open loop comparator is a differential input high gain amplifier with an output stage. A current-mirror acts as the load for the differential pair and converts the double ended circuit to a single ended. Since precise gain is not required for comparator circuit, no compensation techniques are required[4]. Figure 4 shows a self-biased open loop comparator. Schematic of the circuit implementation and simulation result shows that self-biased open loop comparator has better speed of operation compared to latched comparator. The simulation results are tabulated below in table 1. Thought there are two capacitors in open loop comparator resulting in more power consumption, speed of operation and resolution is better compared to latched comparator. So open loop comparator circuit is selected for the design advancement. Both the comparator design is done based of a specific output current and slew rate.

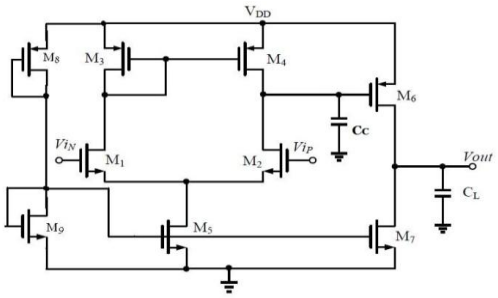

Fig 4 Self-biased open loop comparator

	Conversion time	No of transistors	Resolution	Power
Latched comparator	426.6ns	11	4mv	80nw
Self-biased open loop comparator	712.7ns	10	15mv	58nw

Table 1 Comparator simulation results

[3] DAC ARCHITECTURE

A. R-2R DAC

The digital data bits are entered through the input lines (d0 to d(N-1)) which is to be converted to an equivalent analog voltage (Vout) using R/2R resistor network[5]. The R/2R network is built by a set of resistors of two

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values, with values of one sets being twice of the other. Here for simulation purpose 1K and 2K resistors are used, there by resulting R/2R ratio. Accuracy or precision of DAC depends on the values of resistors chosen, higher precision can be obtained with an exact match of the R/2R ratio.

B. C-2C DAC

The schematic diagram of 3- bit C2C ladder is shown in figure 4.3 which is similar to that of the R2R type. The capacitor value selected as 20 fF and 40 fF for C and 2C respectively such that the impedance value of C is twice that of 2C.

C. Charge scaling DAC

The voltage division principle is same as that of C-2C[6]. The value of unit capacitance is selected as 20fF for the simulation purpose. In order to obtain precision between the capacitance value parallel combinations of unit capacitance is implemented for the binary weighted value. Compared to C-2C the capacitance area is considerably large.

DAC type	Integral Non-Linearity INL		Differential Non-Linearity DNL		Offset
	Max	Min	Max	Min	
R2R	0	0	0	0	0
C2C	0.1	-0.065	0.1644	-0.0601	0.0025
Charge Scaling	-0.003	-0.0151	0.0048	-0.0032	0.0051

Table.2. INL and DNL of DAC architectures

From the table 2 simulation result shows that R-2R architecture provides the best performance compared to C-2C and charge scaling. The output values from the R2R block absolutely matches with the theoretical output values of a 3-bit Digital to Analog Converter but the output results. So R-2R topology is used in this SAR ADC design. The simulation output of 9-bit R-2R DAC with input changing from 000000000 to 111111111 at every 100ns is shown in figure 5.

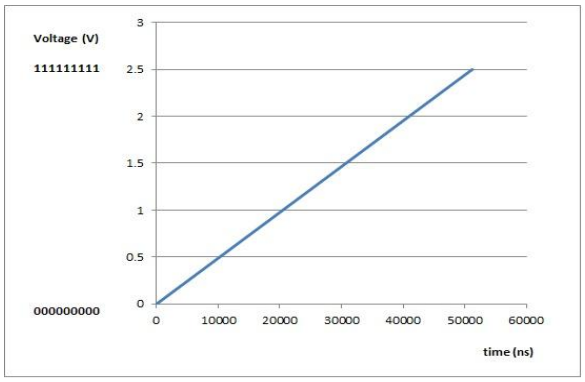

Fig 5 Simulation output of 9-bit DAC

[4] SAR LOGIC

Successive approximation register and control logic can be divided into two stages: sequence generator and successive approximation registers. Sequence generator circuit is implemented using positive edge triggered flip-flops of N+1 numbers and negative edge triggered flip-flops are used for the successive approximation register. An EOC (end of conversion) signal goes high at the N+1th cycle and remains high till the next conversion starts.

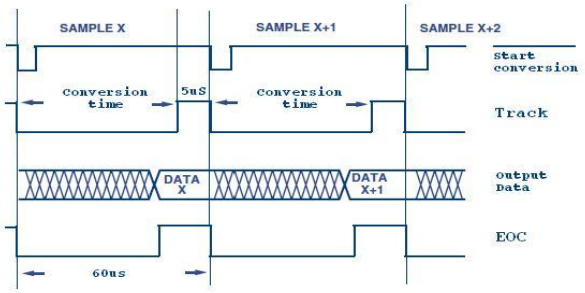

Fig 6 SAR logic timing diagram

The sequence generator produce an output as that of a Johnson counter and successive approximation register stores the comparator output at each cycle according to the control logic. The output of SAR logic is the final ADC output and is same as the input to DAC and hence at the end of conversion, the output of DAC equals to the analog input voltage. The figure 6 shows the SAR logic timing diagram.

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The block diagram of the SAR logic implantation is shown in Fig 7. An internal clock of frequency N times greater than the sampling frequency is used in the logic.

[5] RESULT AND ANALYSIS

The complete design from schematic to GDSII is performed on CADENCE virtuoso EDA tool. Design of the circuit converges to the determination of the aspect ratio of the transistor used in the circuitry. The foundry used here is Tower Jazz semiconductor with 180nm technology in which 3.3 V transistors are used in the design

Acquisition time	305.7ns
Settling time	100.9 ns
Aperture time	98ns
Capacitor leakage	0.616 mV

Table 3 Track and Hold simulation results

Track and hold circuit schematic is simulated with designed instance parameter and the output obtained is shown in figure 8. Sampling signal is 16.7 KHz pulse with 8.16% duty cycle. The signal to be sampled is a sine wave with frequency 1 KHz with amplitude 1.25V and Dc offset 1.25V. The results are tabulated in table 3.

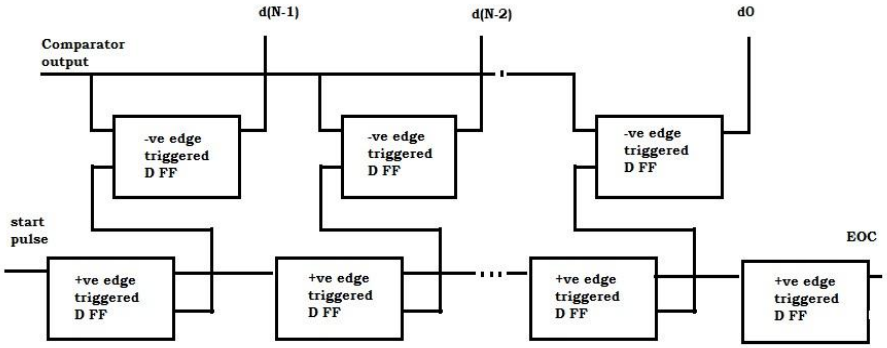

Fig 7 Block diagram of SAR logic

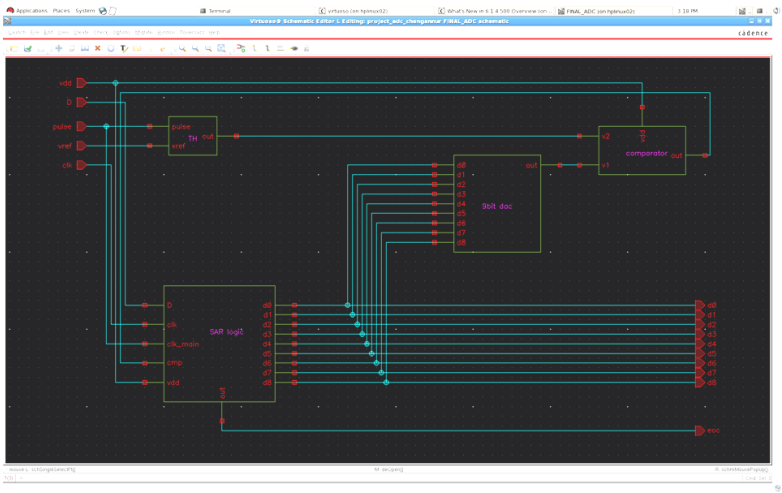

Fig 8 Schematic of final ADC

After the simulation and testing of each block individually, are connected to form the schematic of the final SAR ADC. The schematic of the ADC is shown in figure 6.5. There are five input pins and ten output pins. The input pins and the voltages applied for the simulation is shown below,

clk PULSE (3.3 0 0 0 0 5e-6 6e-6)
D PULSE (3.3 0 0 0 0 2e-6 60e-6)
vdd dc=3.3
vref dc=1.5
pulsePULSE (3.3 0 0 0 0 55e-6 60e-6)

The input to TH is held when the strobe signal is low and the ADC conversion process starts when the start pulse goes high. The output of TH is compared with the output of DAC and the comparison result is stored in the successive approximation register and the process continues till all the nine cycles are completed. The output of DAC converges and become equal to the held input voltage when the end of conversion signal goes high. The

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digital output can be obtained from SAR logic. The output of DAC for the above mentioned simulation conditions are shown in figure 9.

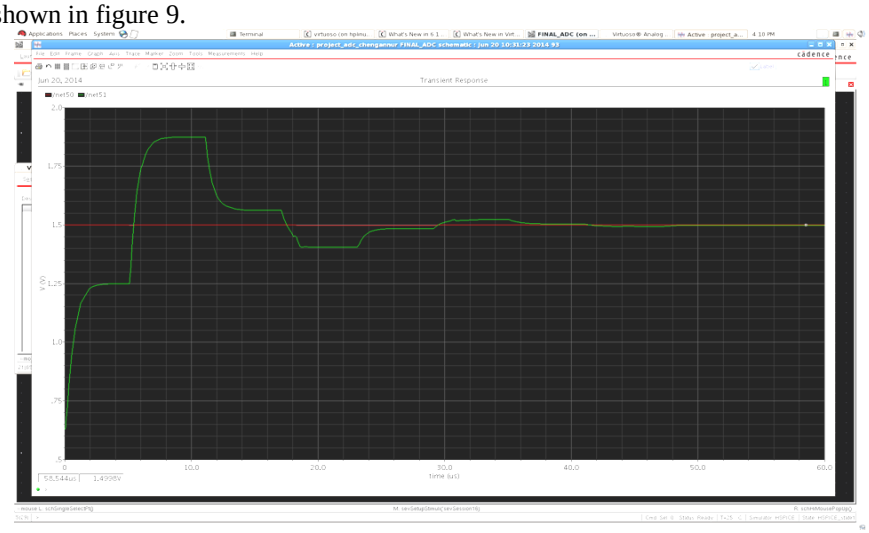

Fig 9 Output of DAC at the end of conversion

The designed ADC has the following specifications

Supply voltage	: 3.3 V
Input voltage range	: 0- 2.5 V
Input current	: 10 mA (Max)
Resolution (N)	: 9
LSB	: 4.882 mV
Architecture	: SAR R-2R DAC
Logic output high voltage (V_{OH})	: 2.4 V
Logic output low voltage (V_{OL})	: 0.5 V
Logic input high voltage (V_{IH})	: 2 V (Min)
Logic input low voltage (V_{IL})	: .8 V (Max)
Conversion time	: 55 uS
Sampling frequency	: 16.67 KHz
Offset error	: < 1 LSB
Gain error	:< 1 LSB
Differential Non Linearity	:< 1 LSB
Integral Non Linearity	:< 1 LSB
SNR	: 58 db
Technology	: 180nm CMOS
Foundry	: Tower Jazz SC

Once the desired response is obtained from the post layout simulation, layout design of the schematic is done. Here layout is drawn in CADENCE Layout XL editor window. The layout designs of individual blocks are drawn and backend design methodologies like placement, routing, etc. are done. The figure 10 shows the layout of a D flip-flop and figure 11 shows the final ADC layout.

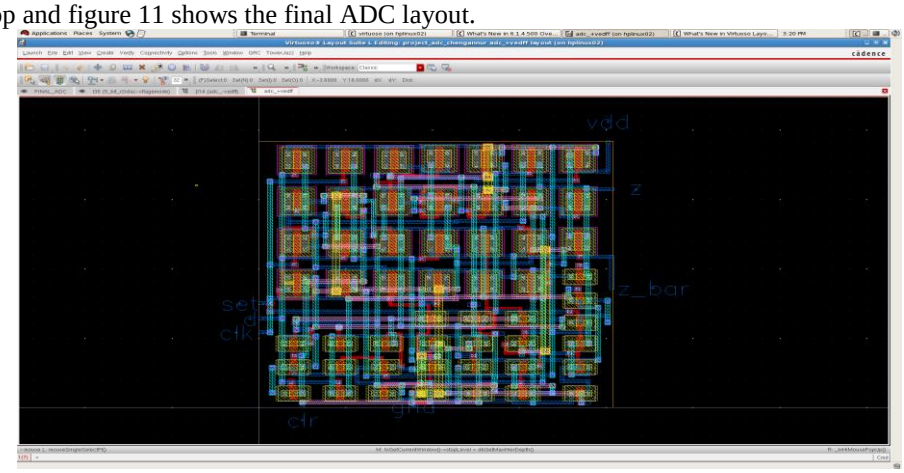

Fig 10 Layout of a +ve edge D flip-flop

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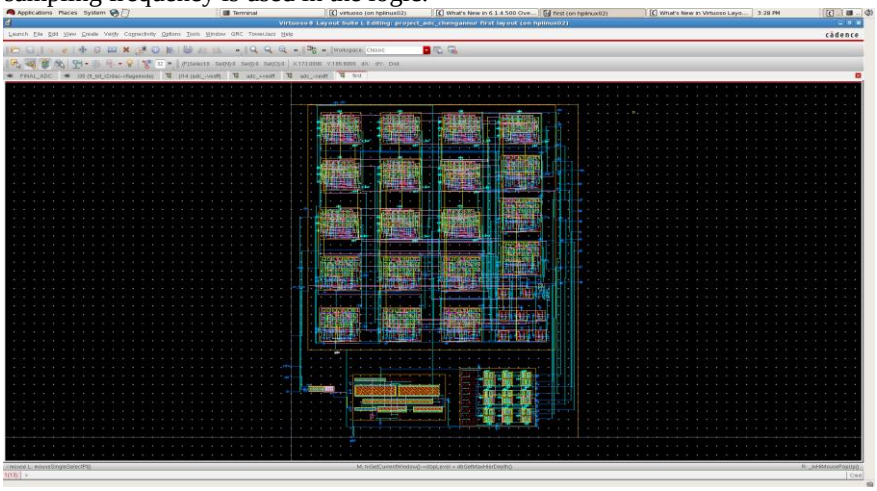

Fig 11 Layout of final ADC

[6] CONCLUSION

In this paper design of a 9-bit SAR ADC design is described and the schematic and layout design provides satisfactory response. The different blocks in the design are implemented using the best topology after a comparative study of the different topologies available. Open loop self-biased comparator provides good resolution and conversion speed of operation. R-2R DAC architecture exhibits the performance comparable to an ideal DAC and has nearly zero INL and DNL. The final ADC schematic is simulated and the conversion time is 55us. The overall power consumption of the circuit is 130mW. The layout of the circuit is drawn in Layout XL editor window of CADENCE EDA tool with area optimization and point-to-point routing technique is used. DRC and LVS checking show zero error and final GDSII extraction is done.

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