HDL Design for Tera Hertz Clock based $2^{23}-1$ Tera Bits per Second (Tbps) PRBS Design for Ultra High Speed Wireless Communication Applications/Products

P.N.V.M SASTRY$^1$, S.VATHSAL$^2$, D.N.RAO$^3$

1Dean-R&D CELL & ECE, Jiginapally B.R Engineering College, Yenkappa, Moinabad, Hyderabad, India
2Dean – R&D & EEE, J.B.Institute of Engineering & Technology, Yenkappa, Moinabad, Hyderabad, India
3Principal – Jiginapally B.R Engineering College, Yenkappa, Moinabad, Hyderabad, India

shastrypnvm@gmail.com, svathsal@gmail.com, principal_jbr@yahoo.com

ABSTRACT
The Design is mainly intended for High Speed Random Frequency Carrier Wave Generator of Tera Bits Per Second Tbps (Tera Bits Per Second) Data Rate using $2^{23}-1$ Tapped PRBS Pattern Sequence. The PRBS is Designed by using LFSR Linear Feedback Shift Register & XOR Gate with Specific Tapping Points as per CCITT ITU Standards. RTL Design Architecture Implemented by using VHDL &/ Verilog HDL, Programming & Debugging done by using Spartan III FPGA Kit. Transmission done through this carrier frequency. Propagation Carrier done either serially / Parallel lines I/O.

Keywords: CCITT – Consulting Committee for International Telegraph & Telecom , ITU – International Telecom Unit, RTL- Register Transfer Level, LFSR-Linear Feedback Shift Register, VHDL- Very High Speed Integrated Circuit Hardware Description Language, PRBS-Pseudo Random Binary Sequence.

1. INTRODUCTION
In Modern Hi-tech Communication Engineering world, High Speed based Portable Communication System Hardware & Software Products Came to the market, speed is an important factor and is in terms of Giga bits per second for all Hi-tech Real time Smart Computing Portable wireless Communication System Software products like Cloud Computing, wireless Internet Data Packets Transceivers Computing, Tablets, Pocket Mobile Multimedia Systems, NoteBook Computers, Wireless Routers, NOCs, Network Cards/Racks, WiFi, WiMAX, GPS, GSM, QCDMA Transceivers. For that purpose, I Designed Giga Bits Per Second, Tera Bits Per Second & Peta Bits Per Second High Speed PRBS is Pseudo Random Binary Sequence Frequency Generators, Generate & Received Random Frequency Data in the form of Random frequency numbers of different speed w.r.t specific data tapping sequence points for both signal & carrier wave generation. PRBS Generators, Receivers, Transceivers Designed for Hi-Fi Wireless Internet Data Bands Computing and Cloud Computing etc. Transmission, Reception of Data is in the RANDOM Sense, This PRBS Generator, Receiver is Designed for Identification property of Different Tapped PRBS Sequences like 7, 10,15,23,31 at a Clock carrier frequency speed of Gbps/Tbps/Pbps.the Length of PRBS sequence is $2^k-1$. $2^k-1$ times repeated the sequences. This is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS, GIS, GSM Communication Systems, WiFi, WiMAX, LTE, Wireless OFDMA, CDMA, QCDMA Computing, wireless internet computing, cloud computing etc because of Ultra High Speed Communication Rate in terms Gbps/Tbps/Pbps. All these PRBS LFSR Sequences are designed by tapping different points according to ITU O.150, O.151, and O.152 Standards. This PRBS Design Consists of Multiplexer, PRBS Registers of different tapped sequence points, Clock Frequency Generators of Gbps/Tbps/Pbps Speed. The Advantages of these PRBS Generators having In Built Checkers, Bit Error Rate Detection & Correction by using PRBS Checkers. These are simply Linear Polynomial Checkers & CRC.

![Figure1](http://ijves.com)

Figure[1]: Fibonacci (many-to-one) realization of LFSR with minimum number of taps and XOR gate in its feedback.

For bit error rate measurements several different PRBS sequences are used. Two standard ones are compared in light of synchronization capabilities: PRBS $2^{17}-1$ (7-bit shift register with taps 6 and 7) and $2^{23}-1$ (23-bit shift register with taps 18 and 23), both generating maximum length sequences. The different types of PRBS and the suggested data-rates for the different PRBS types are described in the ITU-T standards O.150, O.151, O.152 and O.153.
1.1 Tera Bits Per Second (Tbps) PRBS SEQUENCES OF DIFFERENT PATTERNS OF DIFFERENT FREQUENCIES

<table>
<thead>
<tr>
<th>PRBS TYPE</th>
<th>STANDARD</th>
<th>SUGGESTED DATA RATE (Kilo Bits Per Second)</th>
<th>FEED BACK TAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>2^7-1</td>
<td>ITU-T O.150</td>
<td>14.4</td>
<td>7.6</td>
</tr>
<tr>
<td>2^10-1</td>
<td>ITU-T O.150</td>
<td>64</td>
<td>10.3</td>
</tr>
<tr>
<td>2^15-1</td>
<td>ITU-T O.150</td>
<td>1544, 2048, 6312, 8448, 32064, 44736</td>
<td>14, 15</td>
</tr>
<tr>
<td>2^23-1</td>
<td>ITU-T O.150</td>
<td>34368, 44736, 139264</td>
<td>18.23</td>
</tr>
<tr>
<td>2^31-1</td>
<td>ITU-T O.150</td>
<td>28, 31</td>
<td></td>
</tr>
<tr>
<td>2^48-1</td>
<td>ITU-T O.150/151/152</td>
<td>52, 47</td>
<td></td>
</tr>
<tr>
<td>2^63-1</td>
<td>ITU-T O.150/151/152/153</td>
<td>59, 63</td>
<td></td>
</tr>
</tbody>
</table>

1.1.1 Description:
PRBS Generator Design Generates Very Ultra High Frequency (Tera Hertz) Random pattern Sequences called “Seed words” in repeated patterns of length 2^{23}-1 Cycles. This Tera PRBS mainly used in Data Encryption standard coding. Estimation of Speed in terms of Tera bits per second with respect to Tera Hertz Clock Oscillator/Generator. This PRBS suit for Ultra High Speed Wireless System Applications and products like 3G, 4G Wireless, WIFI, GPS, Cloud, Cluster wireless Computing, Big Data Control Centre Stations etc. This PRBS Generator main applicable in wireless Transmitter and Receivers for Data Encryption and Decryption. Carrier and Signal Generators are Designed Based on this Tera Bits Per Second (Tbps) PRBS 2^{23}-1 Sequence Pattern. This PRBS Generates both Carrier and Signal of 2^{23}-1 sequence patterns, these two are correlated with each other and generates Tera PRBS 2^{23}-1 modulated Sequence Pattern Signal.

2. 2^{23}-1 Tbps PRBS Design Architectures

2.1 Tbps Clock Rate Generator

![Fig.1. Tera Hertz Clock Oscillator / Generator (Tbps Clock Rate)](image)

2.1.1 Description: Tbps Clock Rate Generator

This Clock Generator Generates Tera hertz Clock Frequency, This Clock Generator / Oscillator contains Clock Frequency Digital Counter / Divider Generates Tera Hertz Clock out. Clock Frequency Digital Counter generates Single clock of periodicity time of 2^{40} / 2 Cycles for Clock Low and High for Generation of Tera Hertz Clock (Tbps Rate Speed) and Coding Done By VHDL and Verilog HDL.

2.2 2^{23}-1 Tbps PRBS Design Architecture

![Fig.2. 2^{23}-1 Tapped - Tera PRBS Design - Tbps Rate](image)

2.2.1 Description: 2^{23}-1 Tapped - Tera PRBS Design

The Tbps 2^{23}-1 Tapped PRBS Generator Design consists of 32 Bit Data Length based Linear Feedback Shift Register and Tbps Clock Oscillator / Generator. This 32 Bit LFSR Contains 32 Data/ Delay Flip Flop Elements and XOR Gate. Tapping Done by Tapping Points 18 and 23 are compared through XOR Gate and Feed back to the Input of the Register and Generates 2^{23}-1 length Random Repeated Pattern Sequences called “Seed Words” based Encrypted Code Data as per CCITT- ITU O.150/151/152 Standards. All these Seed words are driven by
3. **$2^{23}-1$ Tera PRBS VLSI IC- DESIGN FLOW CYCLE (Software Flow Cycle)**

3.1 Design Flow Description:

Above Figure 3. describes VLSI IC Design Flow, it contains the steps following below, the first step is Initially Entry the Design Specifications of $2^{23}-1$ Tera PRBS Design like I/O Specifications, clock frequency specifications, timing Specifications, Electrical etc. the second step is to Define the Internal RTL Design Architectural Description through RTL HDL Coding either VHDL / Verilog HDL. Third step is simulating the RTL Design and Running the Functionality of the design through Xilinx ISE 9.2 I Design Simulator / Altera Quartus II Model Sim. Fourth Step is Synthesizing the Design in to Gate Level Design through Xilinx FPGA Target IP Core Xilinx XC Spartan III FPGA Soft IP Core. Subsequent steps are Floor planning Placement and Routing done through the FPGA Soft IP Core.

4. DESIGN FLOW REPORTS OF $2^{23}-1$ Tapped Tera PRBS DESIGN (Tbps Rate)

4.1 $2^{23}-1$ Tera PRBS DESIGN RTL BLOCK

---

**IC Design Tape Out**

Fig.3. VLSI Design Flow Chart /Diagram

---

**Fig.4.** $2^{23}-1$ Tera PRBS
4.1 RTL Block $2e^{23-1}$ PRBS

4.2 $2e^{23-1}$ Tera PRBS RTL Schematic

4.3 $2e^{23-1}$ Tera PRBS DESIGN PLACED REPORT

4.4 $2e^{23-1}$ Tera PRBS Routed Design Report
5.0 SIMULATION WAVE FORMS

5.1 $2^{23} - 1$ Tera PRBS Simulation Wave Form

![Fig.9. $2^{23} - 1$ Tera PRBS](image)

5.2 $2^{23} - 1$ PRBS- Simulation Wave Form

![Fig.10. $2^{23} - 1$ PRBS](image)

CONCLUSIONS
The $2^{23} - 1$ Tera PRBS (Tbps Clock Rate) Designed for Ultra High Speed Wireless Communication Engineering Products /Applications like 3G, 4G, WiFi, TiFi, Wireless NOC', Routers, and Cloud, Grid, Cluster, Internet High Speed Data Computing and Future Enhanced Smart Computing Ultra High Speed Wireless Communications. The Design mainly intended for Providing High Speed Communication Tera bits per second Speed of Transmission and Reception of Data Packets / Frames compared to current trends of technology.

REFERENCES
5. Xilinx Data Sheet XAPP884 (v1.0) January 10, 2011

AUTHORS BIOGRAPHY
Software Industrial MNC’s, Corporate –CYIENT (INFOTECH), ISITECH as a world top keen IT Industrial Software Specialist – World Top Software Engineering Team Leader(Level 6) Eng-Eng-HCM Electronics Vertical & Program Manager – MFG I/C, EDS, BT, NON BT Embedded Software, Avionics & Automotive Hi-tech Software Engineering Verticals & Departments, Program Lead – Embedded & VLSI & Engineering Delivery Manager – IT Semiconductor Software Engineering Vertical at ISITECH, also worked with Govt R&D, Industrial Organizations, Academic Institutions of Comparative Designations & Rolls. His Areas Of Interest are VLSI – VHDL, Verilog HDL, ASIC, FPGA & Embedded Software Product Architectures Design & Coding Development. He mentored & Architecting Various Real Time, R&D, Industrial Projects/Products related to VLSI & Embedded System Software & Hardware. His Key Achievements are Participated Various Top Class International IT MNC Delegates Board Meetings, IT Software MNC Board Meetings(Tier1/2 Level MRM-VP, COO Level), Guided R&D, Industrial, Academic Projects/Products – VLSI-ASIC, FPGA & Embedded & Embedded, VLSI Software Project & Program Management & Also Coordinated Various In House & External IT Project Workshops & Trainings At CYIENT(INFOTECH) as a I/C- MFG Eng Software Vertical. Also Participated Various National R&D Workshops, FESTS, FDP’s & Seminars. Recently He Published Various National & International Journals.

Dr. Srinivasan Vathsal obtained B.Tech-EEE in 1968 from Madras University. He got M.E in EEE from BITS Pilani in 1970. He Obtained Ph.D. from School Of Automation, I.I.S.C, and Bangalore in 1974. He Did Two Year Post Doctoral Research in DFVLR, Germany & NASA Goddard Space Flight Centre, USA. Under NRC NASA research fellowship for another two years. He has closely worked with Dr. A.P.J Abdul Kalam in Project SLV of Vikram Sarabhai Space Centre for four years in the mission analysis group. On return from USA he worked in DRDL, Hyderabad as Scientist E, F & G, also Head of Non Destructive Evaluation Division, and officer In-Charge-Joint Advanced Technology Program, Indian Institute of Science. He also worked with Various Academic Institutions as a Professor, Dean of Science & Humanities & Director Energy Centre for One Year. He has worked as Principal of Bhaskar Engineering College, Hyderabad, for 2-years. Currently he is Professor & Dean (R&D)-JBIET, Hyderabad. He has published 80 Technical papers in national & international journals & conferences. He is chief Editor of international journal Intelligent Automation (JIIA), from Korea. He is Chief Editor of JBIET Research Review which is JBIET quarterly Journal. He is life senior member of IEEE. He is fellow IETE and Aeronautical society of India. He is also life member of System society on India, Instrument society of India and Astronautically Society of India. Recently he delivered Invited lecture in University of Minnesota, Minneapolis USA on Application of Kalman filtering for Power Electronics and Power systems. He has guided 5 Ph.D students and currently guiding 8 Ph.D students.

Dr. D.N Rao B.Tech, M.E, Ph.D, Principal of JBREC, Hyderabad. His carrier spans nearly three decades in the field of teaching, administration, R&D, and other diversified in-depth experience in academics and administration. He has actively involved in organizing various conferences and workshops. He has published over 11 international journal papers out of his research work. He presented more than 15 research papers at various national and international conferences. He is Currently approved reviewer of IASTED International journals and conferences from the year 2006. He is also guiding the projects of PG/Ph.D students of various universities.