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High Performance Carry Skip Adder using Reversible Logic

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ABSTRACT

The increasing demand for low-power VLSI can be addressed at different steps of VLSI design cycle, such as the architectural, circuit, layout, and the process technology level. At the circuit design step, considerable potential for power saving exists by means of proper choice of a logic style for implementing circuits. The is because all the important parameters governing power dissipation- switching capacitance, transition activity, and short-circuit currents-are strongly influenced by the chosen logic style. The carry-skip adder reduces the time needed to propagate the carry by skipping over groups of consecutive adder stages, is known to be comparable in speed to the carry-look ahead technique while it uses less logic area and less power. We will design 8-bit Carry Skip Adder by using T-Spice v13.0 for 1v, 90nm technology.

Keywords: *Low power, Carry Skip Adder, logic design style, Reversible Logic, CMOS, Pass Transistor Logic.*

[1] INTRODUCTION

The complexity of microelectronic circuits, power dissipation, delay and area has come the primary design goal with the increasing level of device integration and the growth [1] [2]. The failure mode of high-power circuits relates to the increasing popularity of portable electronic devices. Laptop computers, pagers, portable video players and cellular phones all use batteries as a power source. To extend battery life, low power operation is desirable in integrated circuits. Depending on the area, delay and power requirements, several adder configurations such as ripple carry, carry look ahead, carry-skip, and carry select are available in the literature. The ripple carry adder (RCA) is the simplest adder, but has the longest delay because every sum output needs to wait for the carry-in from the previous adder cell. It uses O (*n*) area and has a delay of O (n), for an n-bit adder. The carry look-ahead adder has delay *O* (log *n*) and uses *O* (*n* log *n*) area. On the other hand, the carry skip and carry select adders have *O* (√*n*) delay and uses *O* (*n*) area. Carry skip adders also dissipate less power than other adders due to their low transistor counts and short wire lengths [3].

2. LITERATURE SURVEY

In recent VLSI Systems [1] [2] the power-delay product becomes the most essential metric of performance. The reduction of the power dissipation and the improvement of the speed require optimizations at all levels of the design procedure. Since, most digital circuitry is composed of simple and/or complex gates; we study the best way to implement adders in order to achieve low power dissipation and high speed. CMOS circuit design styles and Reversible logic style is given, describing their advantages and limitation. Also, various design and implementation of Carry Skip Adder were analysed in terms of delay and power consumption using T-Spice. Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation. Quantum arithmetic components need reversible logic circuits for their construction. Reversible logic circuits find wide application in low power digital design, DNA computing and nanotechnology. In 1960 R.Landauer [4] demonstrated that high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. According to Landauer's principle, the loss of one bit of information dissipation kTln2 joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed. Later Bennett [5] [6], in 1973, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible logic.

3. ARCHITECTURE OF CARRY SKIP ADDER

Carry Skip Adder (also known as Carry Bypass Adder) is an adder implementation that improves on the delay of a Ripple Carry Adder with little effort compared to other adders. The improvement of the worst-case delay is achieved by using several carry-skip adders [7] [8] to form a block carry skip adder. The carry skip adder provides a compromise between a ripple carry adder and a CLA adder. The carry skip adder divides the words to be added into blocks. Within each block, ripple carry is used to produce the sum bit and the carry.

The Carry Skip Adder reduces the delay due to the carry computation.

• If each Ai # Bi in a group, then we do not need to compute the new value of Ci+1 for that block; the carry-in of the block can be propagated directly to the next block.

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• If Ai = Bi = 1 for some i in the group, a carry is generated which may be propagated up to the output of that group.
• If Ai = Bi = 0, a carry, will not be propagated by that bit location. The basic idea of a carry-skip adder is to detect if in each group all Ai # Bi and enable the block's carry-in to skip the block when this happens. In general a block-skip delay can be different from the delay due to the propagation of a carry to the next bit position [7] [8].

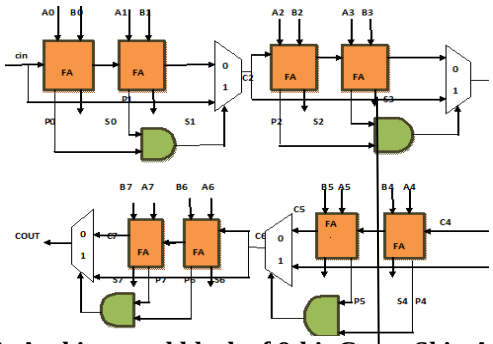

Fig.1. Architectural block of 8-bit Carry Skip Adder

4. LOGIC DESIGN STYLES

At the circuit design step, considerable potential for power savings exists by means of proper choice of a logic style for implementing circuits. This is because all the important parameter governing power dissipation-switching capacitance—are strongly influenced by the chosen logic style. Depending on the application, circuit can be implemented in different logic style.

4.1 Standard CMOS Logic:

It is the most common and widely utilized digital logic in almost any application field. Still, other digital logic styles exist and are utilized in the industry as well. Since we aim in this thesis work for special design characteristics, such as very low power consumption and very small sized designs, it is fair to have a look at other digital logic design styles as well.

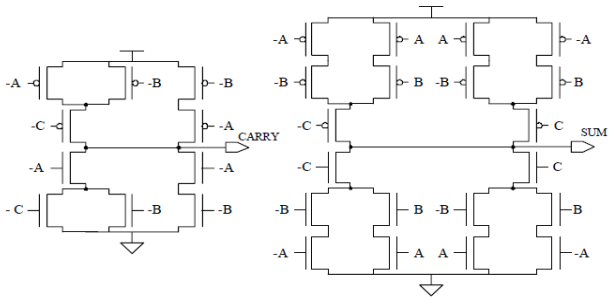

Fig 2. Full Adder using CMOS Logic

The implementation of Carry Skip Adder(CSKA) using CMOS Logic is shown in Fig.3 and its corresponding simulated waveform in Fig.4.

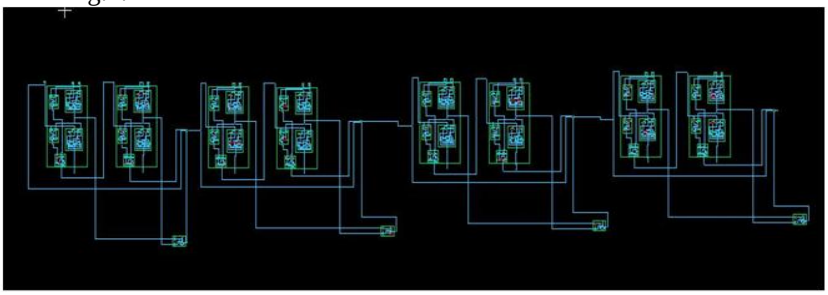

Fig.3. Schematic diagram of CSKA by CMOS Logic

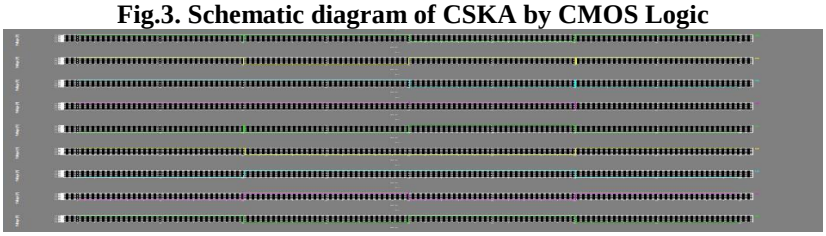

Fig.4. Simulation waveform of CSKA by CMOS Logic

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5. REVERSIBLE LOGIC:

A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. Reversible circuits are constructed using reversible logic gates. These reversible circuits not only produce unique output vector from each input vector but also the input can be reconstructed from the outputs. A reversible circuit should be designed using a minimum number of reversible gates. Fan-out and loops are not allowed in reversible logic circuits. However fan-out and feedback can be achieved by using additional gates. Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation. Reversible logic circuits find wide application in low power digital design, DNA computing, quantum computing and nanotechnology. In 1960 R.Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. According to Landauer's principle, the loss of one bit of information dissipates kTln2 joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed. Later Bennett, in 1973, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits.

The complexity and performance of the circuit is decided on the following parameter.

(i) **Garbage outputs:** The number of unused outputs present in the reversible logic circuit.

(ii) **Number of reversible gates:** Total number of reversible gates used in the circuit.

(iii) **Delay:** Maximum number of unit delay gates in the path of propagation of inputs to outputs. It represents the total number of reversible gates used between the primary inputs and the outputs of a reversible logic circuit.

(iv) **Constant inputs:** The number of inputs which are maintained constant at 0 or 1 in order to get the required function. They are necessary to synthesize a reversible function.

(v) **Quantum cost:** The number of 1x1 or 2 x 2 reversible logic gates used in the quantum equivalent of the reversible circuit.

Toffoli Gate: Fig. 5 shows a 3 x 3 Toffoli gate [10][11]. The input vector is I (A, B, C) and the output vector is O (P, Q, R) and output is defined by P = A, Q = B, R = AB Xor C.

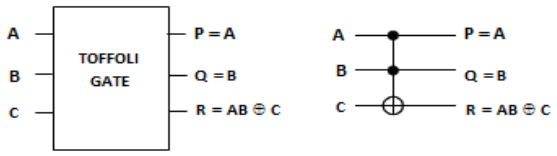

Fig.5. Toffoli Gate and its quantum implementation

Table 1. Truth table of Toffoli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

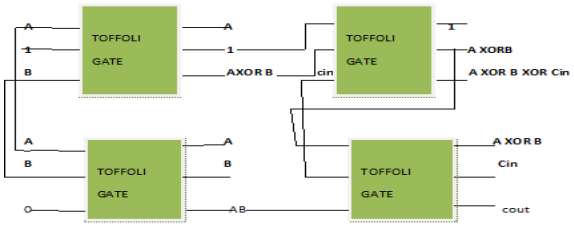

Fig.6. Toffoli gate Full Adder

The implementation of Carry Skip Adder (CSKA) using Pass Transistor Logic is shown in Fig.7 and its corresponding simulated waveform in Fig.8

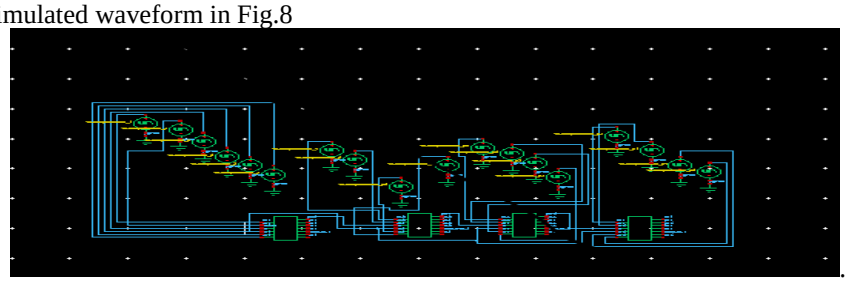

Fig.7. Schematic diagram of 8-bit CSKA using Toffoli Gate(PTL) Full Adder

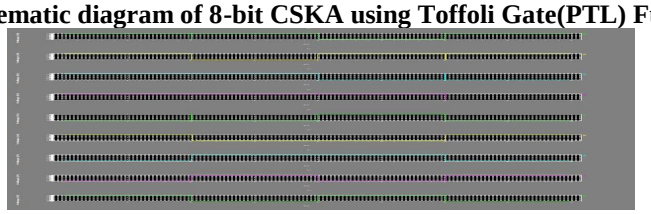

Fig.8.Simulated waveform of 8-bit CSKA using Toffoli Gate(PTL) Full Adder

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The implementation of Carry Skip Adder(CSKA) using CMOS Logic is shown in Fig.9 and its corresponding simulated waveform in Fig.10

Fig.9. Schematic diagram of 8-bit CSKA using Toffoli Gate (CMOS)Full Adder

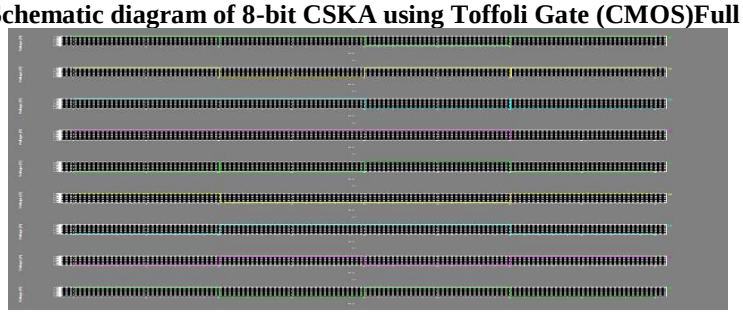

Fig.10.Simulated waveform of 8-bit CSKA using Toffoli Gate(CMOS) Full Adder

PERES GATE: The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A xor B and R=AB xor C. In the proposed design Peres gate [12] [13] is used because of its lowest quantum cost.

Table 2. Truth Table of Peres Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

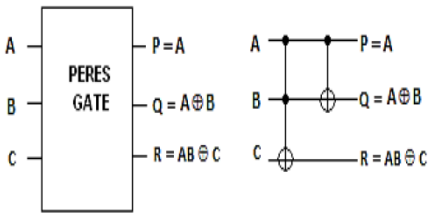

Fig.11.peres Gate and its quantum implementation

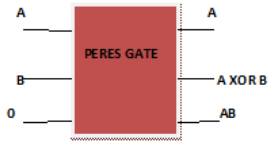

Fig.12.Peres Gate implementation of AND2 and XOR2

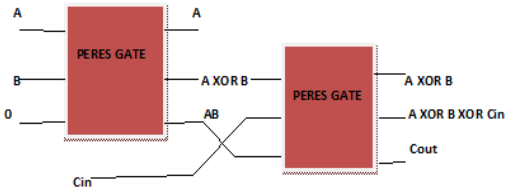

Fig.13.Peres gate Full Adder

The implementation of Carry Skip Adder(CSKA) using Peres Gate CMOS Logic is shown in Fig.14 and its corresponding simulated waveform in Fig.15.

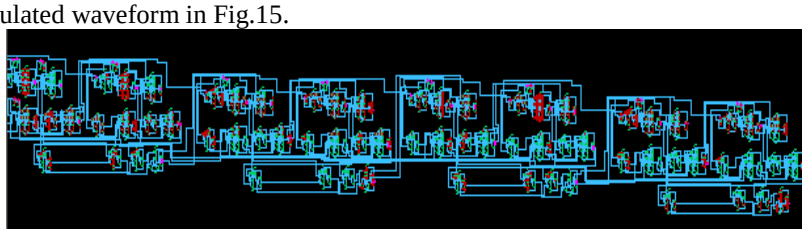

Fig.14. Schematic diagram of 8-bit CSKA using Peres Logic(CMOS) Full Adder

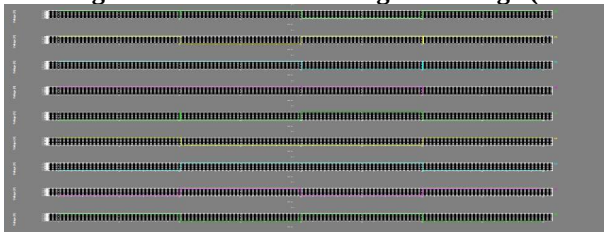

Fig.15.Simulated waveform of 8-bit CSKA using Peres Gate (CMOS) Full Adder

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The implementation of Carry Skip Adder(CSKA) using Peres Gate Pass Transistor Logic is shown in Fig.16 and its corresponding simulated waveform in Fig.17.

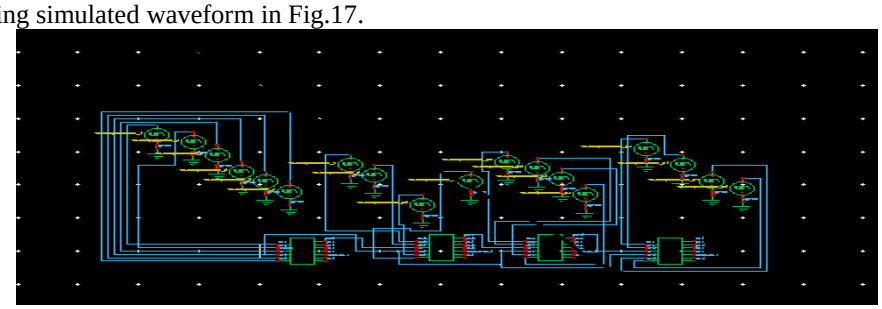

Fig.16. Schematic diagram of 8-bit CSKA using Peres Logic(PTL) Full Adder

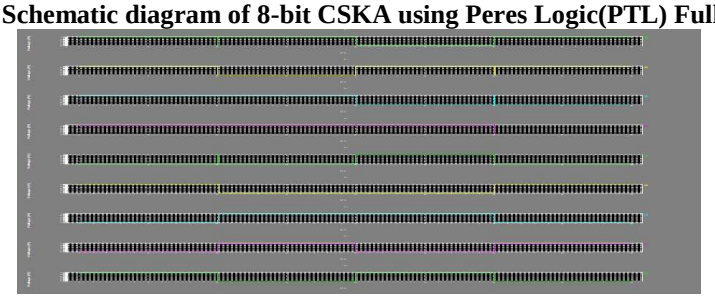

Fig.17.Simulated waveform of 8-bit CSKA using Peres Gate (PTL) Full Adder

6. PERFORMANCE PARAMETER AND SIMULATION SETUP:

The 8-bit Carry Skip Adder is compared based on the performance parameters like propagation delay, number of transistors, power dissipation and garbage output . To achieve better performance, the circuits were designed using Static CMOS logic process technology and Reversible logic process. The channel width of the transistors is 450n for the NMOS and 900n for the PMOS and the channel length is 150n with Vdd 1 volt. All the circuits have been designed using TANNER EDA with Model file as **dual.md**. The power estimation is a difficult task because of its dependency on various parameters and has received a lot of attention. Direct Simulation method is used in order to analyse the results.

Table3. Shows Comparative Experimental results of Carry Skip Adder using different Logic Styles in terms of area, power and delay

Logic style	Power dissipation(mw)	Propagation delay(ns)	Powerdelay product(PDP)(pJ)	No. of transistor	Garbage output
Peres CMOS	1.01	89.46	90.35	548	8
Peres PTL	0.22	35.89	7.89	66	8
Toffoli CMOS	0.11	16.88	1.85	560	56
Toffoli PTL	0.22	11.49	2.52	120	56

Comparison of 8 bit CSKA using different logic Styles(PeresCMOS, PeresPTL, ToffoliCMOS, ToffoliPTL) in power dissipation(mw), power delay(ns), no. Of transistor, power delay product(PDP) are shown in Fig.18.

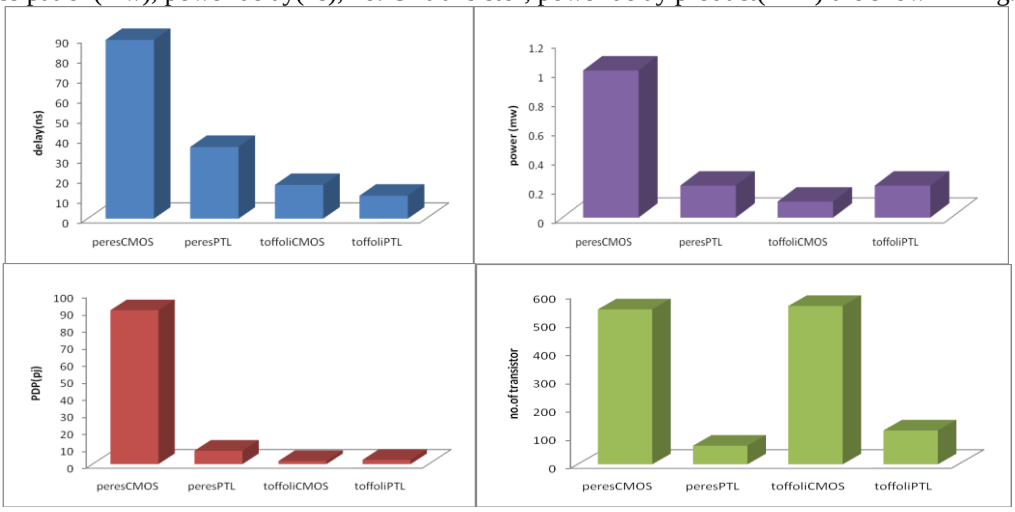

Fig.18. Comparison between different logic style in terms of delay, power, PDP and no. of transistor

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7. RESULT ANALYSIS:

It has been observed that Reversible logic using Peres gate Full Adder and Toffoli gate Full Adder exhibit better characteristics (speed and Low-Power) as compared to other design styles. So, Reversible logic style can be used where portability and high speed is the prime aim. Where, Reversible logic using gates consumes the lowest power. With the reduction of Garbage Output, Reversible logic can be considered best logic design style with respect to all parameters of 8-bit Carry Skip Adder architectures.

8. CONCLUSIONS

We have designed and simulated 8bit CSK adder using different logic style in T-Spice V13.0. Here, an optimized Carry Skip adder using Reversible logic gates is presented. The design is very useful for future computing techniques like ultra low power digital circuits and quantum computers. The advent of reversible logic will significantly contribute in reducing the power consumption. The design method is definitely useful for the construction of future computers and other computational structures. Optimization of other computational circuits is under investigation as a future work.

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