Vol 06, Article 01526; January 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

FPGA BASED WIRELESS SENSOR NETWORK NODE: SURVEY

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ABSTRACT

Wireless Sensor Networks represent one of the most prominent technologies in recent years. In WSN node architectures, the increasing complexity and high number of intensive tasks of today's higher-end applications limits the use of traditional ultra-low power microcontrollers having sufficient but limited computational capacity and low scalability. The high performance high capacity FPGA based WSN node architectures provide the advantages of the intrinsic acceleration due to hardware parallelism, the use of partial reconfiguration capabilities for changeable environments, as well as a careful power aware management techniques for energy savings. This paper analyses different research prototypes available on FPGA based Wireless Sensor Network nodes and gives an understanding in this technology.

Keywords: *Wireless Sensor Network; FPGA; Soft core of FPGA; Partial reconfiguration*

[1] INTRODUCTION

In the last few years Wireless Sensor Networks (WSNs) have drawn the attention of research community due to its wealth of practical challenges in utilization of an efficient form of technology that has no structures or rules or adhering to a specific standard. These WSNs are expected to be autonomous low power demanding, context aware and flexible for number of applications such as; military, health monitoring, indoor and outdoor firefighting applications, security applications, and environmental, agricultural, climate changes and studying animal behavior. Also, due to its portability, it may be carried out on everywhere from the human body to be deeply embedded in the environment.

In WSN, there is tremendous need for energy-efficiency as the sensors nodes have the extreme energy constraints to operate for years with the energy budget of a small battery. Also another important criterion is flexibility making its design an extremely challenging task, as there exist a wide spectrum of different application scenarios for WSN, varying strongly in their characteristics complexity in assessing different parameters such as data rates, wake-up intervals, Network topologies, etc., hence system requirements.

The use of microcontrollers in classical design approaches for WSN node provides a good trade-off between programming flexibility, price and size. However, the combination of efficiency and small size on one hand and flexibility on the other hand is very difficult to realize on these classical architectures. As compared to being more flexible, microcontrollers can be energy inefficient due to high complexity time when faced with very intensive tasks. Better solution can be achieved by using DSPs as compared to standard microcontrollers in reduction of computational time but it is still very high, to maintain the energy efficiency of WSNs. Alternately, ASICs can provide most energy-efficient solution, but lack flexibility and utilize high design cost and time, at least in the prototype stage.

Reconfigurable hardware can be a new design approach to fill the gap in the design space between these (two) extremes. Research studies in the last years have provided Reconfigurable systems as an alternative for both (ASIC) Application Specific Integrated Circuits and (GPP) General Purpose Processors. GPPs, for instance suffer an imbalance between input-output and processing. Differently fine-grained reconfigurable device such as FPGA provide not only a large amount of IO's, but also high processing due to parallelism and pipelining. When applications are characterized by high throughput data i.e. video or audio sensors, additional devices like FPGAs are required. Recent works show that FPGAs are valuable candidates for data signal processing in WSN. Flexibility and performance efficiency of FPGAs are interesting characteristics for high end applications WSN nodes. Re-programmability, re-configurability, performance and effective hardware/software codesign are powerful features of FPGA-based systems which makes the FPGA-based WSN node energy and performance aware platforms. The rest of the paper is organized as follows: Section 2 highlights the different research prototypes of WSN node based on FPGA. Section 3 evaluates different design architectures of FPGA based WSN nodes by some technical features such as target technology, dynamic partial reconfiguration, energy efficiency, implementation technology and modular architecture. Section 4 concludes this paper. And finally last section cites the references for this paper.

2. RELATED WORK

A WSN node is composed of sensors, actuators, a network interface, power supply unit (batteries, external, solar, etc.) and a processing unit. In case the digital signal processing requirements are high (such as for high

Vol 06, Article 01526; January 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

throughput sensorial information), additional processing units are required. Currently state-of-the-art sensor nodes for smart networks are capable of processing data at node end before transmitting to base station, having compact size, reduced power consumption, low cost and most important minimum manual intervention. In this section we outline some of this related work.

In [1], the authors present a re-configurable WSN node. The node is implemented on Altera's cyclone II FPGA integrated with a soft core processor NIOS II focusing on mixed development based on hardware/software codesign. In [2], the authors present a FPGA based wireless vision sensor node. The architecture includes a microcontroller and an Altera EP2C35 FPGA to provide low-power hardware Image compression. In [3] the hyperchaos encryption engine is developed on a Spartan 3E FPGA prototype board which acts as a high performance coprocessor attached to an external ZigBee transceiver. The paper [4] presents a prototyping platform for an SRAM FPGA based safety related communication system for a wireless sensor network, where, as a case study an acceleration sensor application is introduced. This architecture mainly consists of an FPGA-based 1oo2 (one out of two) architecture which is implemented as two 8 bit microprocessor (Intel 8051) integrated into a single FPGA.

Similarly, architecture for dynamic reconfiguration of advanced WSN node is presented in [5]. The authors illustrate how dynamic reconfiguration can be achieved on Flash-FPGA devices. A recent work in the field of Wireless Multimedia Sensor Networks (WMSN) [6] takes advantage of FPGAs to implement an improved CSMA/CA mechanism for IEEE 802.15.4 protocol to allow reliable and timeliness transmission of voice data. The architecture has been tested on a Xilinx Spartan-3E FPGA, performances results are presented but energy consumption is not taken into account.

The design approaches mentioned above results certain benefits in terms of flexibility or performance by including re-configurable devices in WSN. However leave important issues such as power consumption, power management or the initial of sensor devices, among others. By contrast, the development of a complete FPGA based node is provided in [7] having modular structure called Cookie platform similar to presented in [8].

Overall we can see from the current literature that most of the research is focused on developing smart sensing nodes for WSN. The next section evaluates these node architectures.

3. EVALUATION

In this section we compare the design of FPGA based WSN nodes proposed by number of research groups. The comparison is broadly classified based on following technical features:

- Target Technology
- Dynamic Partial Reconfiguration
- Energy Efficiency
- FPGA Implementation Technology
- Modular Architecture of FPGA based Nodes

3.1 Target Technology

In This section the number of nodes are evaluated based on whether FPGAs are used to perform signal processing only (in this case an external microcontroller is required), or to manage both signal processing and operating systems (a soft core on the FPGAs).

Figure 1 shows the two scenarios:

- The top of the Figure 1 shows, the microcontroller is external to the FPGA.
- The second in Figure 1 shows, the microcontroller is implemented in FPGA. This solution offers more flexibility with respect to the first. Thanks to this architecture, the FPGA can be process the information from sensors, (or the control for the actuator) completely in parallel. In fact, a dedicated IP core can be written for each sensor (or actuator) in order to exploit the performance of FPGA.

3.1.1 Nodes Based on External Microcontroller

In [9], the authors present the implementation of FPGA based Wireless Sensor Node with a simulated chemical plant distributed process monitoring application by using collaborative clusters of wireless sensor nodes. The sensor node measures and pre-processes the raw data from sensor source before sending them to a higher order node in the network in order to achieve real time monitoring. This node consists of sensor, ADC, MSP4301F1612 Microcontroller (μC) which is the heart of the node and Xilinx Spartan 3 FPGA as the secondary processor to increase efficiency in WSN by taking computational load off the main processor. The idea to use FPGA in the node is to get analog data from external sensor board and pre-process this data to lower amount of information required for Wireless transfer and thus ensuring maximum uptime of the WSN node. The paper [10] presents a novel partial dynamic reconfiguration (PDR) image sensor node prototype for WMSN to solve the problems of limited resource and large amount of image data to be processed and transmitted and providing security while transmitting sensitive images in WMSN node. In this paper FPGA is adopted to accelerate data processing and JPEG image compression algorithm with less power consumption in WMSN node. Also partial dynamic reconfiguration system is designed for the sensor node to acquire multiple

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http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

compression ratios and to enhance the safety by working with AES encryption. This WMSN consists of five components: data processing, wireless transmission, image sensor, frame buffer and power supply. The data processing component of node consists of a STMicroelectronics µC and Xilinx Spartan 3E FPGA. The µC is the core element for the control of the system. It is in charge of receiving and transmitting files and deals with FPGA reconfiguration.

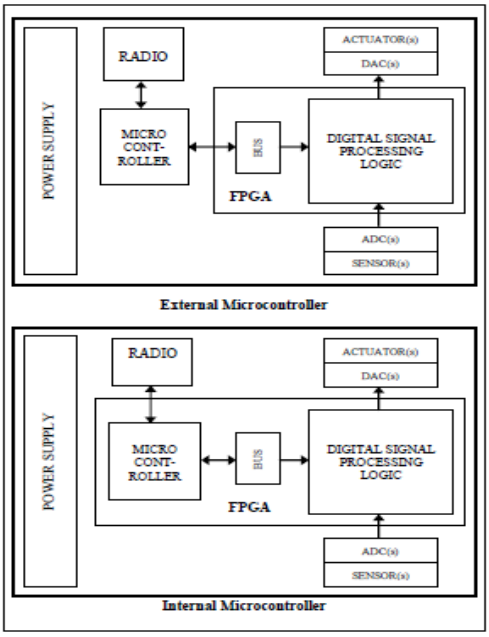

Fig.1. An FPGA-based WSN node. In both cases, FPGA is used for digital signal processing. In the first case, an external microcontroller is used to manage radio communication and the operating system. In the second case, the microcontroller is implemented into the FPGA [17]

3.1.2 Nodes Based on Soft Core of FPGA

As mentioned in section II, paper [1] proposes a new hardware/software Interface synthesis design method aiming at the 32-bit NIOS based SOPC platform on Altera's cyclone II FPGA with a dynamically re-configurable functional units. The functional architecture consists of four units; data acquisition unit, a treatment unit, a routing unit and a radio integrated unit. Dynamic reconfiguration is implemented for two intensive energy efficient computational tasks to minimize the energy required for the communication. Firstly, to minimize the energy consumption, the information related to the measured data is transmitted only in case there is a considerable amount of change with respect to base data, not always and secondly, the energy efficient protocol LEACH (Low energy adaptive cluster hierarchy) is used for the transmission of data from node to the base station using shortest path.

In [11], Altera's cyclone FPGA device, equipped with a configurable NIOS II soft core is used as a sensor node with the main features of the WSN are reconfigurability, programmability and scalability. The proposed network protocol is implemented in the NIOS soft core RISC processor with all the peripherals and because of its programmability feature, the sensor node can be easily adapted for many data sensing applications. Addition or removal of the nodes can be done easily without disturbing the existing configuration and no manual configuration is required. Also, the above mentioned paper [3] in section 2, the WSN node design is completed with 32-bit Microblaze soft-core as primary processor combined with the basic hardware circuit configuration on FPGA development board as the core processor and the ZigBee protocol for communication. The transported data in the network is encrypted using hyperchaos encryption by FPGA, which combines the flexibility in rapid real-time data processing with free configuration in FPGA and enhances the security of the transported data.

3.2 Dynamic Partial Reconfiguration

Taking all the different applications and protocols into account, a large variety of functions can be found in the domain of wireless sensor networks. Amongst them are error detection and correction schemes, encryption and authentication, data compression, aggregation and preprocessing, media access, routing, and others. Naturally, each of them can be realized with different algorithms, and which alternative performs best usually depends on many factors. The ability to implement all required algorithms efficiently is the key challenge to get an adaptive system that can combine energy-efficiency and flexibility without wasting a large amount of chip area. A promising solution to meet this goal is to re-use hardware resources through dynamic partial reconfiguration [1]. Partial Reconfiguration (PR) provides a method to reconfigure selected regions of the FPGA while the remainder of the device remains active. The FPGA is partitioned into two or more partially reconfigurable

Vol 06, Article 01526; January 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

regions (PRRs) plus one static region that does not change. In contrast to full FPGA device configuration, which requires *full bitstreams* (configuration data for the entire device), PR capable FPGAs use *partial bitstreams*, allowing to specify only the configuration data for a particular PRR.

The paper [12], explains that an FPGA based system that considers multiple modules is more difficult to design than a microprocessor based system. Since WSN environments are dynamic in nature, the quantity and type of targets may change frequently, requiring many system reconfigurations – *situation-based reconfiguration*. Thus, *modular systems* are required to provide flexibility with respect to executing module quantity and type. One potential solution creates many predefined module mixes for different situations and a bitstream (i.e., FPGA configuration file) for each situation. Choosing an appropriate module mix is non-trivial, as the number of combinations is exponential. Additionally, FPGA runtime reconfiguration between different module mixes interrupts execution. Fortunately, partial reconfiguration (PR) in FPGAs addresses many of these limitations [13]. PR enables selective region reconfiguration without system disruption. This module isolation reduces bitstream storage and communication requirements, since only the data associated with the particular PRR is required. This paper presents that the most significant PR benefit is PRR reconfiguration without halting execution of entire device. This isolated reconfiguration is beneficial when critical system tasks such as communication links, timers, managers, etc. must remain operational at all times. In the case of WSNs, active modules could be tracking critical targets and should not be halted while loading new modules. The authors in this paper developed VAPERS (Virtual Architecture for Partially Reconfigurable Embedded Systems) architecture for PR- capable FPGAs to provide a flexible and dynamic module communication layer, regardless of module location, size, or clock domain. The VAPRES central controlling agent orchestrates module loading and unloading, which involve making runtime decisions on when to place a module inside the PRRs (online scheduling) and which specific PRR implementation to use (online placement).

In paper [14], the authors explained the main advantage of exploiting partial reconfiguration in embedded devices, like WSN nodes, apart from the reconfiguring much smaller configuration files than complete ones is that it also produces lower memory and bandwidth requirements. In this paper, the FPGA partial reconfigurable system has been built based on *Virtual Architectures (VAs)* that integrate both the resource division and the on-chip communications (the on-chip interconnections of different FPGA regions). Here run-time reconfiguration support is applied to three different functions: i) the sensor hardware interfaces; ii) the coprocessor allocated in the FPGA for taking advantage of the HW parallelism; and iii) the µC-to-FPGA interface. Thus, the selected approach provides a solution that exploits partial reconfiguration capabilities of the FPGA included in the Cookie, in order to increase flexibility, reduce the amount of data transmitted and reduce the reconfiguration time. As mentioned above in section 2, the paper [10] presents a partial dynamic reconfigurable (PDR) WMSN node. As shown in Fig. 2, the JPEG image compression algorithm is implemented on-board in a partial reconfigurable way, in order to enhance safety and reduce the reconfiguration files. It is composed of several modules where some JPEG encoder blocks are static modules and quantization block and Huffman encoder block are partial reconfigurable modules. When a Partial reconfiguration file is needed, quantization table or Huffman table is changed according to the demand thereby changing the compression ratio and partial reconfiguration files are regenerated. The experimental results of this architecture shows that PR files are only 12% of the whole configuration files. Although this proposed PDR is slower than ASIC but it is much more flexible than ASIC.

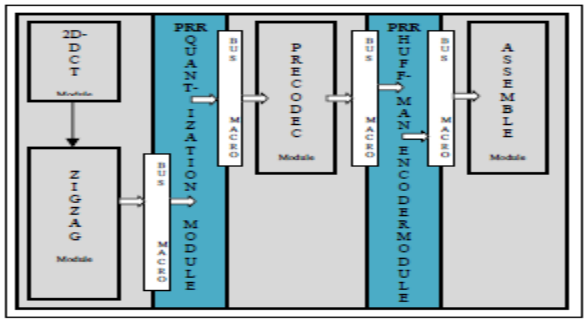

Fig.2. Reconfigurable JPEG Encoder Architecture [10]

3.3 Energy Efficiency

The Energy Efficient Consumption in WSN node is always one of the major challenges for designers because of limited powered battery. The more energy is saved, the more node lifetime is extended. In this scenario, power consumption of WSN is a critical constraint, and the nodes must be designed to make an efficient use of the available energy to sense, process and transmit the information.

As mentioned in section 3.1, paper [1], the dynamic configurable sensor node was developed for energy efficient computational intensive tasks to minimize the energy required for communication. Also, in section 3.1, paper [9], the limitation of the WSN node is that it requires a DC power source due to FPGA power constraints.

Vol 06, Article 01526; January 2015
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International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

FPGA draws certain sustainable amount of power in order to operate stably**.** Thus, a more complicated circuit to solve higher initial power consumption of FPGA is needed. Also, the authors in paper [15] achieved high power efficiency in the proposed HiReCookie structure node by applying the very efficient power management strategies which are controlled by an external AVR microcontroller.

In [16], the authors implemented a high-performance node based on SRAM-based FPGA for WSN by applying power management techniques which is explained below. Here the authors explained a typical power consumption profile of the RAM-based FPGA node. Three regions are differentiated: sleep period, reconfiguration period, and computing period. The power management techniques described in this paper focus on the reduction of the current consumption during three periods explained in sections 3.3.1, 3.3.2 and 3.3.3. Also, it is concluded in this paper that, with a flat mAh battery, there would be sufficient energy for almost 279,000 reconfiguration cycles in the best case (not accounting FPGA degradation).

3.3.1 Sleep period

Some Wake-up policies and sleep modes have been implemented to reduce power consumption during this inactive period of time. The results show that the consumption during sleep modes could be less than 2mA.

3.3.2 Configuration period

There are two different methodologies to decrease power consumption during this period:

- By increasing the configuration clock frequency: *Every time the system is powered, the FPGA starts to generate addresses to read the bitstream file from the external memory. At the beginning the configuration frequency is set to 1 MHz by default. Then, when the FPGA starts to read the bitstream file, this frequency can be increased upto 6MHz by editing the header of the configuration file.*
- By reducing the size of bitstream file: *In order to optimize this reduction, the next three steps were followed; first is by relocation of HW modules using the PlanAhead Tool in order to maximize the empty areas, second is by compressing the bitstream file using the commands given by Xilinx, and third is reducing the bitstream file by erasing the empty areas, that is, extracting a partial-initial bitstream rather than using a complete one.*

3.3.3 Computing period

To reduce the high current consumption during execution period. The main idea in this stage is to compensate the high current with very fast calculations, so that the energy is finally reduced i.e. using advantage of HW acceleration and parallel HW.

The paper [17], presents a controller to manage energy consumption in Flash-based FPGAs systems. Dynamic energy consumption, evaluated on a real case study with a real testbench, shows overall energy consumption of the FPGA lower than 4mW with high sampling rates, which allows the system to work with batteries. In this proposed architecture authors have used IGLOO family Flash-based FPGA manufactured by Microsemi, as it not only supports *Active* and *Shutdown* modes but also supports *Sleep* mode with Flash*Freeze technology. The *Sleep* mode allows the system to reduce the power consumption of the device by switching off all the input/output signals of the FPGA including clock and reset. Energy aware applications require system architectures to be able to directly and effectively control the *Sleep* mode at runtime. To reach this objective an Intellectual Property (IP) called *Sleep IP* is developed which is able to manage the FPGA during the *Sleep* mode, allowing the system to go into *Active* mode after a predefined period of time. Microsemi IGLOO FPGAs are equipped with an internal digital pin called *Freeze* Pin, which allows the system to enter the *Sleep (Freeze)* mode when the pin is set to one, and to exit when the pin is set to zero. The proposed Sleep IP and the complete system architecture implemented on the Flash-based FPGA are intended to be generic and reusable in many WSN applications.

3.4 FPGA Implementation Technology

Memories used to store data and configuration information, dispersed on the FPGA, can be created using SRAM or Flash technology. In SRAM FPGAs, data and configuration are stored into volatile memories whose content is lost when the device is power-off. On the other side, Flash FPGAs store the information in non-volatile memories, thus the content is kept even if the device is power-off.

Table 1 shows the analysis of pros and cons of SRAM and Flash FPGAs presented in paper [17].

Here the authors have considered the following three power modes:

- Active: *FPGA is working at full speed. This mode provides maximum power consumption and performance.*
- Sleep: *clock and I/O ports are turned off, the internal state is maintained but the device is o.*
- Shutdown: *the FPGA is powered-off. In this mode, the power consumption of the device is zero.*

A SRAM FPGA must be completely reconfigured after each power-up, due to volatility nature of memories, causing a waste of time and power. One of the main drawbacks of SRAM FPGA is that the reconfiguration is the most power consuming activity, and another drawback is that the time needed to reconfigure the complete device takes several milliseconds. Thus, making a reconfiguration on each start up unfeasible when data are sampled at medium/high frequencies. Although SRAM-based FPGAs cannot compete in terms of static power consumption with other FPGA technologies, like the non-volatile ones, the increased flexibility provided by the possibility of dynamically and partially reconfigures them, as well as the higher resource availability, may make

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ISSN: 2249 – 6556

these RAM based FPGAs good candidate solutions for high performance applications. In this way, the purpose of the work presented in [15] is to show the power management techniques that are applied to a custom designed node architecture with an SRAM FPGA, so that the main drawback of excessive energy consumption is minimized.

Recent Flash based FPGAs can be considered as the second generation of FPGAs; overcoming the limits of non-volatility of previous SRAM-based FPGAs, Flash-based FPGAs are promising in low-power, real-time applications. The ability to preserve the LUTs configuration after a shutdown, known as live at power-up, perfectly fits battery powered systems, where the device can be entirely shutdown to preserve energy. Thus, the work presented in [17] provides an evaluation of Flash-based FPGAs technology for novel WSN's nodes. Differently from SRAM-based FPGAs, thanks to Live at power-up, Flash-based FPGAs allows the system to effectively control the power consumption of the system at runtime. As explained in detail in section 3.3, here the authors have used the power features of novel Microsemi IGLOO devices, and from the experimental results it is observed that the power consumption of the FPGA can be kept below 4 mW even with high sampling rates.

Table 1. SRAM vs. FLASH FPGA [17]

	PROS	CONS
SRAM	•Fast programmibility •Small configuration bit-streams •High Performance •High chip density	•Need to be programmed on each power-up •High power consumption
Flash	•Live at power-up •Low static power consumption •Efficient power control mechanism	•Low chip density •High cost

3.5 Modular Architecture of FPGA Based Nodes

In [8], a modular structure for the WSN node is proposed which is composed of four layers: sensing, processing, communication and power supply layer as shown in Figure 3:

- Sensing Layer: *It includes conditioning circuits for both digital and analog sensors. The output signal of these conditioning circuits goes through the vertical connectors to the processing layer.*
- Power supply layer: *It is the power source of the node. The node can be powered from an USB cable, lithium or AA batteries or directly from the mains if it is necessary.*
- Communication layer: *It includes the radio module to communicate data between nodes. It can be either a ZigBee or a Bluetooth module.*
- Processing layer: *It is the brain of the platform. It is the layer in charge of processing all the information given by the sensors and the radio module. It includes a low-cost and low-performance Spartan 3 FPGA, together with an external microcontroller.*

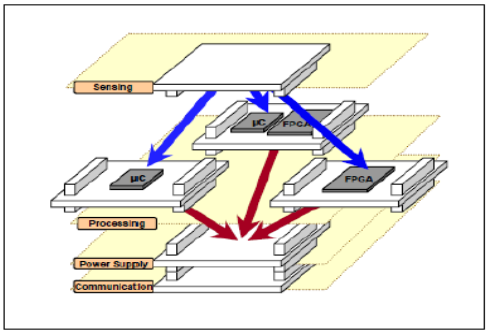

Fig.3. An Illustration of modular Structure of WSN Nodes [8]

In [7], the robust, miniature, wireless sensor network node is fabricated using modular structure approach and with an area of 25mm x 25mm. The aim of 25mm sensor cube is to provide a novel 3-D programmable modular system that could be used as a toolkit for ambient systems research (such as robotics, autonomous agents and neural networks, telemetry, transducer networks, etc.). The key properties of the node are modularity, robustness, functionality and compactness. In [14], the original Cookie platform is featured with complete runtime reconfigurable system that has been defined and designed for the FPGA included in the node. Here the Cookie node reconfigurability is associated not only with loading new SW programs in the microcontroller (SW reprogramming), but also new HW configurations in the reconfigurable fabric (HW reconfiguration). In [15], an integrated design of an SRAM FPGA based high performance node including not only a high performance FPGA, but also power management and monitoring circuitries, external memories and conditioning circuitry for external sensors is proposed. Besides, power management strategies and a dynamic and partial reconfiguration mechanism are also proposed, integrating efficiently dynamic reconfiguration features within the node. In [16], the power consumption techniques implemented in a high-performance node for WSN based on SRAM based

Vol 06, Article 01526; January 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

FPGA intended for high-end WSN applications that include complex sensor management like video cameras, high compute demanding tasks such as image encoding or robust encryption, and/or higher data bandwidth needs.

CONCLUSION

Both WSNs and FPGAs independently have been popular research topics, but their combination is an emerging and challenging field, and thus there exists few research prototypes. New and innovative higher-end WSN applications demand longer battery life, faster responses, and high performances. FPGAs, and in particular PR-capable FPGAs, provide a logical next step to satisfy these demands by providing a great balance of performance, parallelism, cost, and power.

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