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LOWPOWER ANALYSIS OF FLP-FLOP USING GDI TECHNIQUE

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ABSTRACT

This paper explains about the logic style comparisons based on different flip-flop functions and Gate Diffusion Input logic (GDI).Power dissipation is an important parameter in the design of VLSI(Very large scale integrated) circuits, and the network of clock signal is responsible from a substantial part of it. Low Power digital CMOS becomes more and more essential, in the general advances process technology and due to new low power applications. As technology advances push for smaller devices operation is fast and less power consumption and become severe problems when designing high-speed ICs. This technique is appropriate for designing of fast, low power circuits, using reduced number of transistor in the improvement of power consumption.

Keywords: Low power, Power minimization, Logic Gates, GDI Technique, Layout, Micro wind.

I. Introduction:

A new implementation of efficient Flip-Flop using Gate-Diffusion-Input (GDI) technique is presented. The FF design allows reducing power-delay product and area of circuit, with the maintenance of low complexity of circuit logic design. Performance comparison with other DFF design techniques is presented, with respect to number of devices and power dissipations of GDI Flip-flop, as compared to other methods [1]. A variety of circuits have been implemented to compare the proposed GDI structure with existing alternatives, showing reduction in power-delay product in GDI [2]. Low power design has become one of the main concerns in VLSI Design [4]. Of the various building blocks in digital system design. The most complexity in the power consuming system is the flip-flop. This project explains about the different architectures of flip-flops with various CMOS logic families and GDI low power design techniques [5]. As these flip flop topologies have small area and less power consumption, this can be used in various applications like digital clocking system, buffers, registers, microprocessors etc. Performance comparison with traditional CMOS techniques is presented [3].

II. Flip-Flop and Latches:

Generally,in electronics, flip-flop or latch is a circuit that has two stable states and can be used to store state information .The circuit can be made to change state by the signals applied to one or more controlable inputs and will have one or two output states. It is the general basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems. Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal. A comparative analysis of latches and flip-flops commonly used in high performance systems. The Flip-flops can be divided into some types as

1) SR Flip-flop
2) JK Flip-flop
3) D flip-flop
4) T Flip-flop

III. GDI based design:

It is a new technique for low power digital combinational circuit design. This technique reduces power consumption and area of digital circuits while maintaining low complexity of logic design. The main difference between the CMOS and GDI based design is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. This feature gives the GDI cell two extra input pins for use which makes the GDI design more flexible than CMOS design.GDI cell consists of three inputs - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of both NMOS and PMOS are connected to N and P respectively. GDI logic based on different input values. So by using GDI technique we can implement various logic functions with less power as compared to conventional CMOS design.

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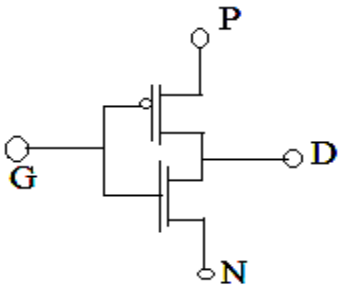
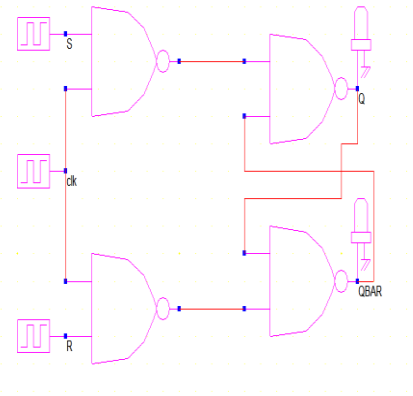


FIG.1 GATE DIFFUSION INPUT (GDI CELL)

IV. Existing flip-flop based on CMOS technique:

1) SR flip-flop



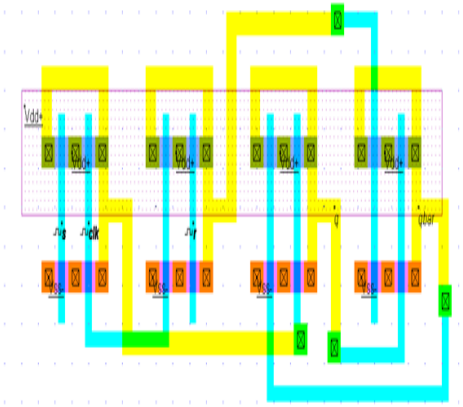


FIG.3EXISTING SR FLIP-FLOP LOGIC DIAGRAM FIG.4 LAYOUT DIAGRAM FOR SR FLIP-FLOP

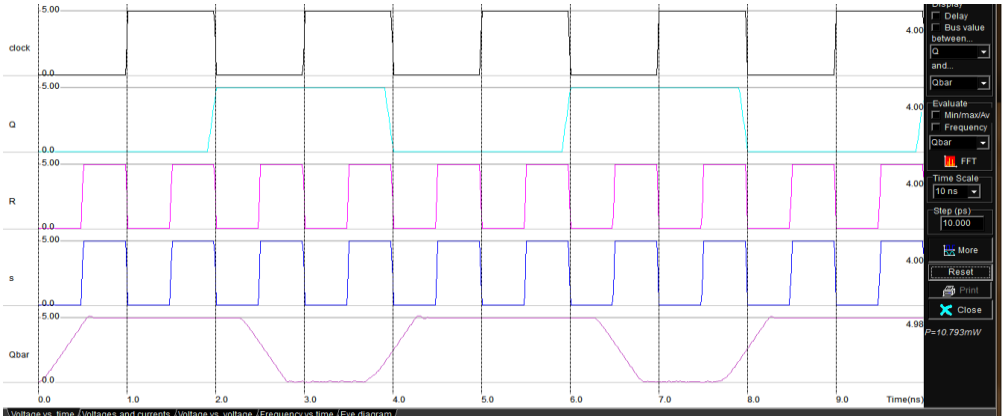
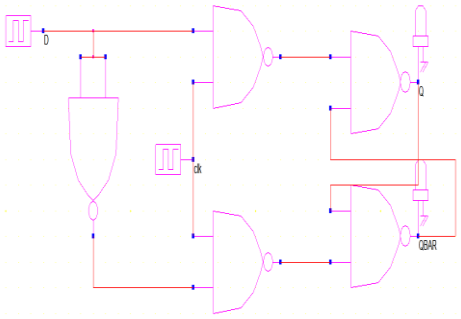


FIG.5 SIMULATION RESULTS FOR SR FLIP-FLOP
CLOCK,S,R-INPUT Q,QBAR-OUTPUT

II)D Flip-Flop:



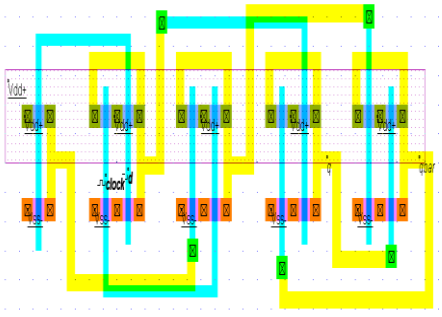


FIG.6 EXISTING D FLIPFLOP LOGIC DIAGRAM FIG.7 LAYOUT DIAGRAM OF D FLIP-FLOP

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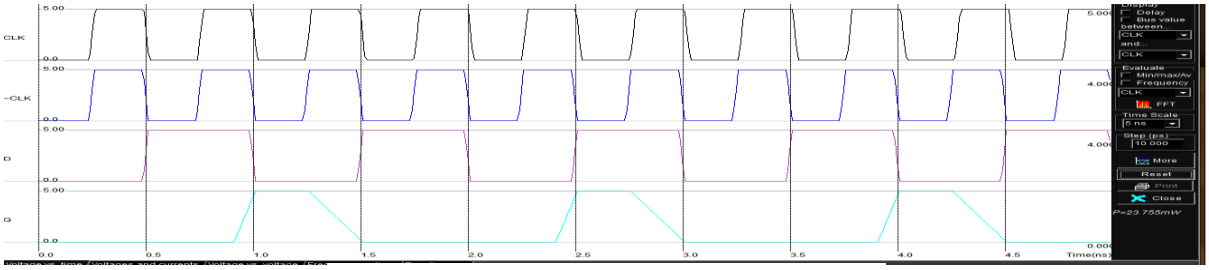
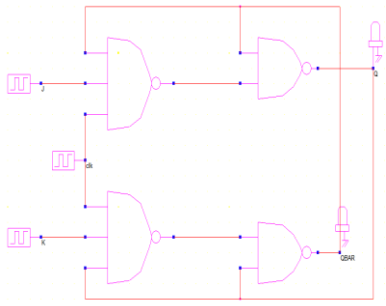


FIG.8 SIMULATION OUTPUTFOR D FLIPFLOP
CLOCK,D-INPUT Q,QBAR-OUTPUT

III)JK flip-flop:



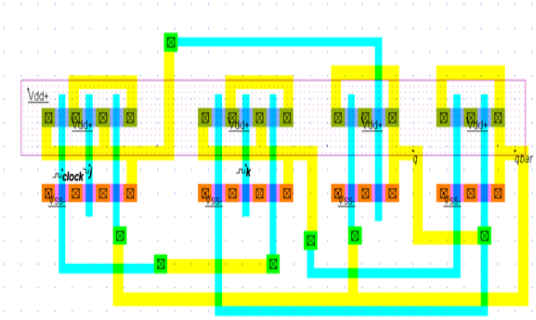


FIG.9 EXISTING JK FLIPFLOP LOGIC DIAGRAM

FIG.10 LAYOUT DIAGRAM OF JK FLIP-FLOP

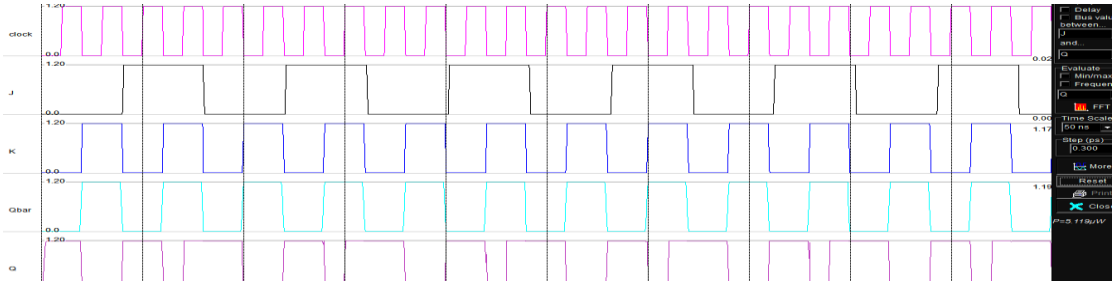
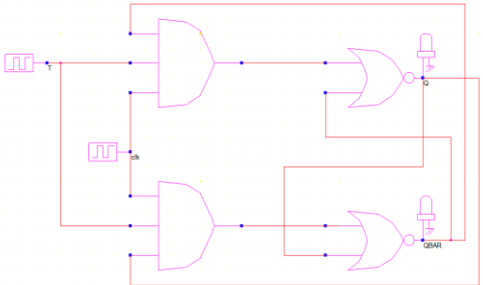


FIG.11 SIMULATION OUTPUT FOR JK FLIP-FLOP
CLK,J,K-INPUT Q,QBAR-OUTPUT

IV)T Flip-Flop:



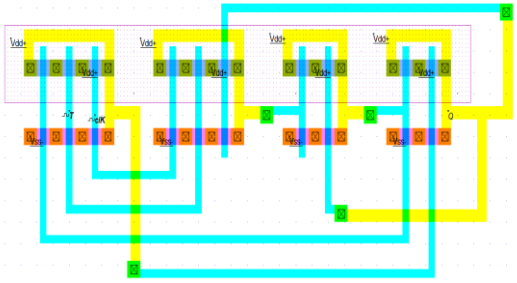


FIG.12 EXISTING T FLIPFLOP LOGIC DIAGRAM

FIG.13 LAYOUT DIAGRAM OF T FLIP-FLOP

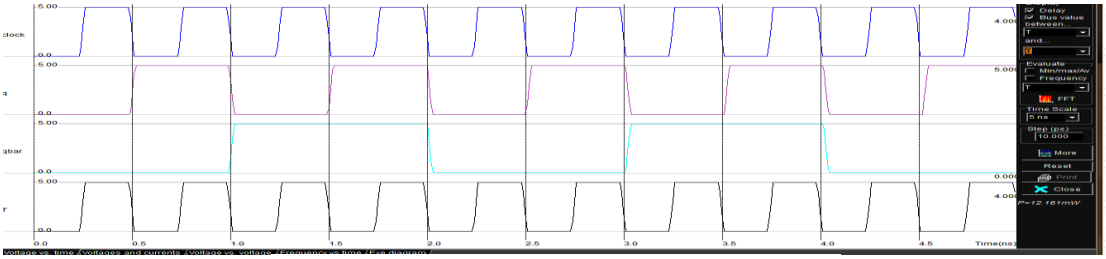


FIG.14 SIMULATION OUTPUT FOR T FLIPFLOP
T,CLK-INPUT Q,QBAR-OUTPUT

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V.Proposed flip flop using GDI technique:

I)SR FlipFlop:

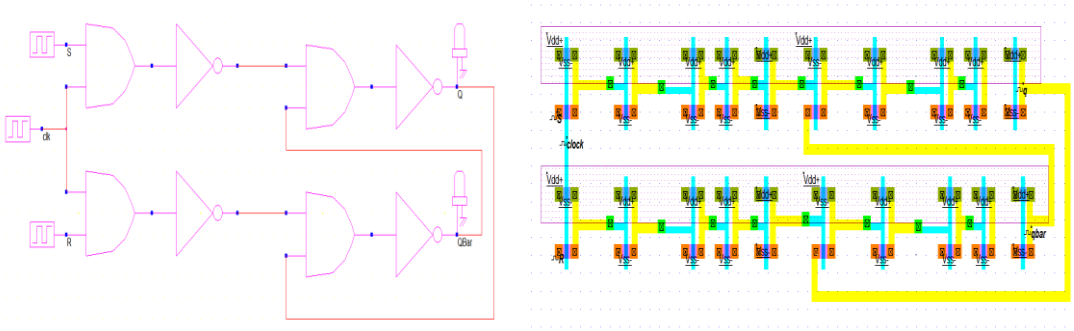

FIG.15 LOGIC DIAGRAM FOR SR FLIPFLOP USING GDI TECHNIQUE
FIG.16 LAYOUT DIAGRAM OF SR FLIPFLOP USING GDI TECHNIQUE

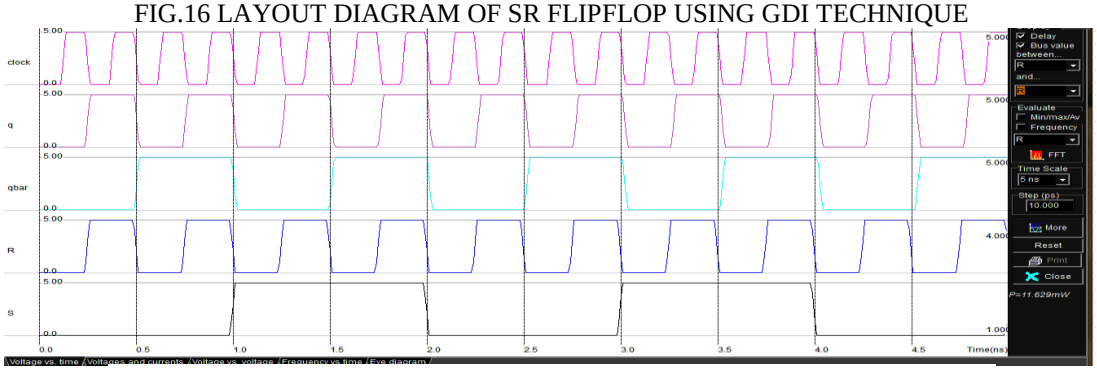

FIG.17 SIMULATION OUTPUT FOR SR FLIPFLOP USING GDI TECHNIQUE
S,R,CLK-INPUT Q,QBAR-OUTPUT

II) D Flip-Flop:

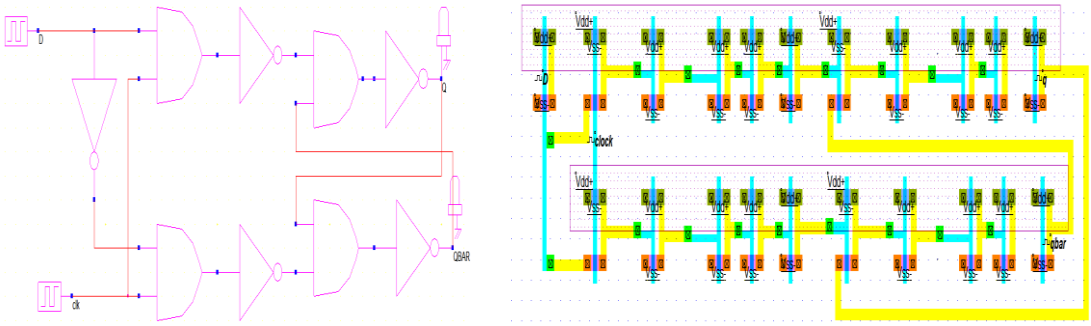

FIG.19 LAYOUT DIAGRAM OF D FLIPFLOP USING GDI TECHNIQUE
FIG.18 LOGIC DIAGRAM FOR D FLIPFLOP USING GDI TECHNIQUE

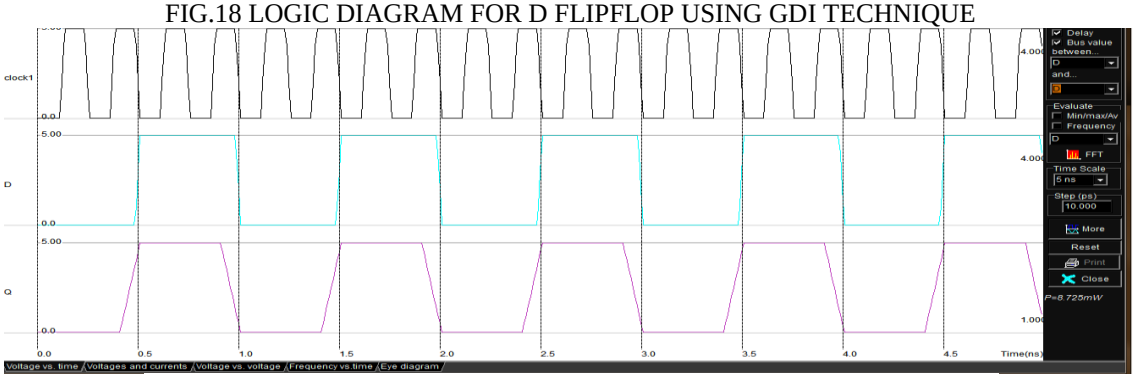

FIG.20 SIMULATION OUTPUT FOR D FLIPFLOP USING GDI TECHNIUE
D,CLK-INPUT Q-OUTPUT

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III) JK Flip-Flop:

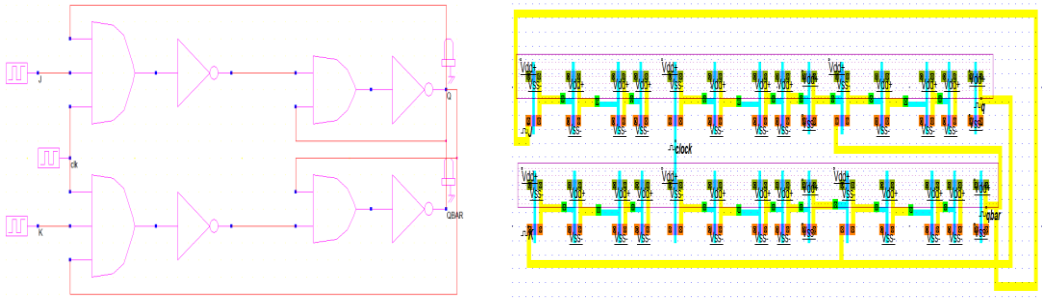

FIG.22 LAYOUT DIAGRAM OF JK FLIPFLOP USING GDI TECHNIQUE
FIG.21 LOGIC DIAGRAM FOR JK FLIPFLOP USING GDI TECHNIQUE

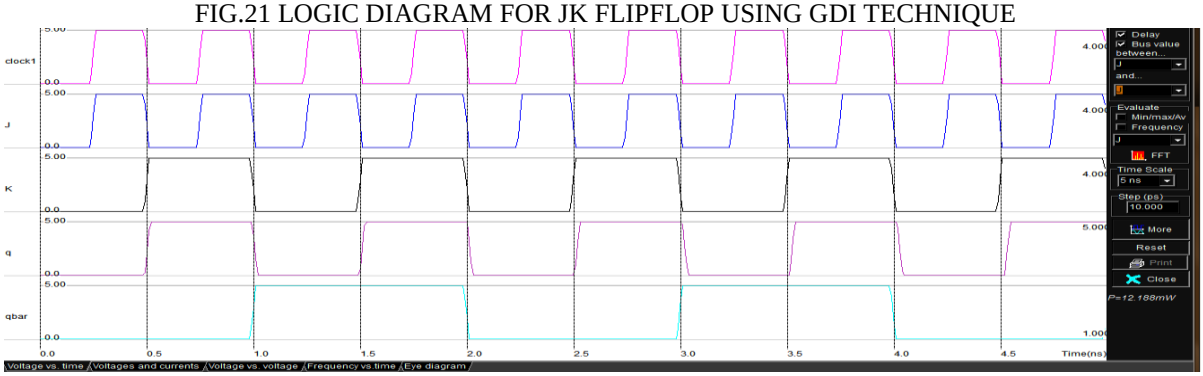

FIG.23 SIMULATION OUTPUT FOR JK FLIPFLOP USING GDI TECHNIQUE
J,K,CLK-INPUT Q,QBAR-OUTPUT

IV) T Flip-flop:

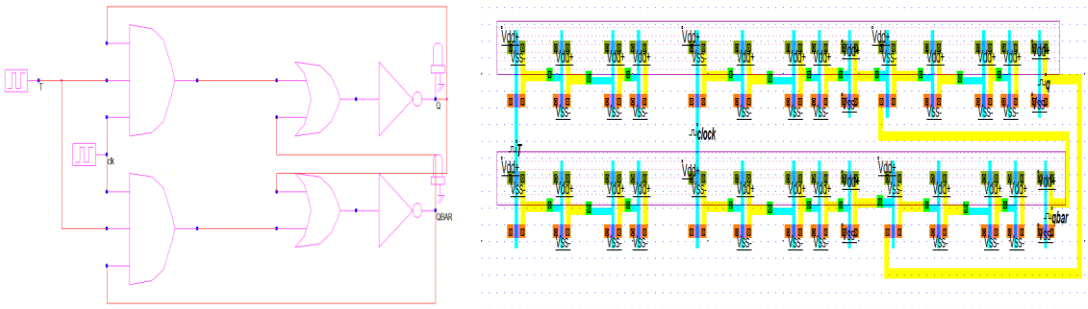

FIG.25 LAYOUT DIAGRAM OF T FLIPFLOP USING GDI TECHNIQUE
FIG.24 LOGIC DIAGRAM FOR T FLIPFLOP USING GDI TECHNIQUE

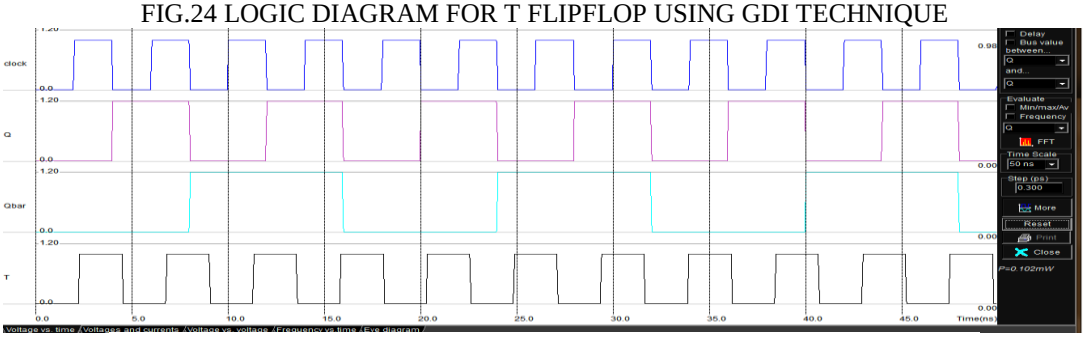

FIG.26 SIMULATION OUTPUT FOR T FLIPFLOP USING GDI TECHNIQUE
CLK,T-INPUT Q ,QBAR-OUTPUT

TABLE I. COMPARISON TABLE OF VARIOUS DEVICES

FLIP FLOP	EXISTING SYSTEM POWER	PROPOSED SYSTEM POWER
SR FLIP FLOP	18.793mW	11.399 mW
JK FLIP FLOP	23.920mW	12.188mW
D FLIP FLOP	10.576Mw	8.725mW
T FLIP FLOP	12.161mW	10.021mW

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Conclusion

Here a detail analysis of average power consumption and delay of proposed GDI based flip-flop and the existing GDI based flip-flop on different technologies is presented. Comparison of proposed GDI technique with the existing GDI technique shows that the average power is decreasing respectively. So by proper analysis of power and delay parameters we can easily use proposed GDI flip-flop over existing flip-flop for low power applications. Implementation of different kinds of mixed and digital circuits have to be carried out in order to determine the fields of circuitry, where GDI is very much superior over other design styles.

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