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PERFORMANCE COMPARISON OF DIFFERENT POWER GATING TECHNIQUES IN AFPL-PCR

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ABSTRACT

This paper exhibits a novel low power logic family, called Asynchronous Fine grain Power gated Logic (AFPL). Each pipeline arranged in the AFPL circuit is comprised of Effective Charge Recovery Logic (ECRL) entryway, which executes the logical functions of the stage and a Handshake Controller (HC), which manages handshaking with the adjacent stages and power up ECRL gates. In the AFPL circuit, ECRL entryways obtain control and get to be dynamic just when performing helpful computations and idle ECRL gates are not triggered and consequently have insignificant leakage dissipation. The Partial Charge Reuse (PCR) mechanism can be incorporated into the AFPL circuit. In PCR mechanism, a part of the charge on the output nodes of an ECRL gate entering the discharge phase can be reused to charge the output nodes of an alternate ECRL entryway going to assess, decreasing the energy dissipation needed to finish the evaluate phase of an ECRL entryway. Additionally, the AFPL-PCR embraces an upgraded Sutherland C-element, called a Sleepy Stack Sutherland C-element, in its handshake controllers such that an ECRL gate in the AFPL-PCR can enter the sleep mode early once its output has been obtained by the downstream pipeline stage. The method of Sleepy Stack technique is comparatively more efficient than the previous techniques adopted. In order to survey the quality of the proposed AFPL, it is incorporated into the application Kogge-Stone adder for further performance comparisons.

Index Terms: *- Asynchronous circuit, Leakage Power, Power gating, Sleep Transistor, Forced Stack*

1. INTRODUCTION

As the feature size keeps on contracting and the corresponding transistor thickness builds, power dissipation has turned into a vital concern Nano scale CMOS VLSI outline. In CMOS circuit, power dissipation can be categorized into dynamic dissipation and static dissipation. The power dissipated when the device is alive is termed dynamic power, and static power is the power dissipated when the device is powered up yet no signals are changing their characteristics. Dynamic power comprises of switching power, brought about by charging and discharging of load capacitance, and the internal power, created by the short circuit current and the current required to charge the internal capacitance of the cell. Static dissipation results from leakage currents, and the essential root of leakage includes sub-threshold leakage, gate leakage, gate induced drain leakage and junction leakage [17]. Based upon the threshold potential, channel length and gate oxide thickness, keep on shriveling up, leakage dissipation is turning into a significant patron to constitute as much as 33% of aggregate power dissipation. A few strategies for reducing leakage, loss in CMOS circuits have been offered both at the circuit and process technology levels [17]. Leakage reduction techniques involved at the circuit level admit transistor stacking [4] [14], reverse body biasing [7] [15], dual threshold CMOS [17] [20] and power gating [5] [15]. From the above techniques, power gating is a standout amongst the most proficient strategies for leakage reduction. By and large, power gating systems expand the powerful safety of leakage ways by introducing sleep transistors (power gating transistors) between power supply rails and transistor stacks. In the static mode, the sleep transistors are turned off, cutting off the pull- up, pull-down networks off from one (or) both power rails, and accordingly leakage current are repressed. In the dynamic mode, the sleep transistors are turned on, reconnecting the pull- up, pull-down networks to power supply rails.

A digital circuit is synchronized on the off chance that its plan includes the utilization of a solitary clock pulse controlling all circuit events. For synchronous circuits, power gating can be experienced in the fine grain orcoarse grain manner. The fine grain approach has more chances to lessen leakage at run time than the coarse grain power gating methodology. However, in that appreciation are a few outline issues connected with introducing fine grain power gating in synchronous circuits. A digital circuit is asynchronous when no clock signal is used to hold in any sequencing of events. These circuits utilize neighborhood handshaking for exchanging data between neighboring modules, so they are data driven and alive just when performing useful computation. Asynchronous circuits can be sorted by the guidelines [11]. Asynchronous circuits don't switch when latent and inherently have the focal point of setting up what might as well be called fine grain clock gating. Although these circuits in idle mode have no dynamic dissipation, regardless they endure leakage dissipation. A few strategies have been proposed for utilizing power gating systems to cut the static power of asynchronous circuits at distinct levels of granularity [14] [17]. Asynchronous circuits can be power gated at the gate level of granularity [9] [2]. In [9], every combinational block in the ordinary asynchronous four phases

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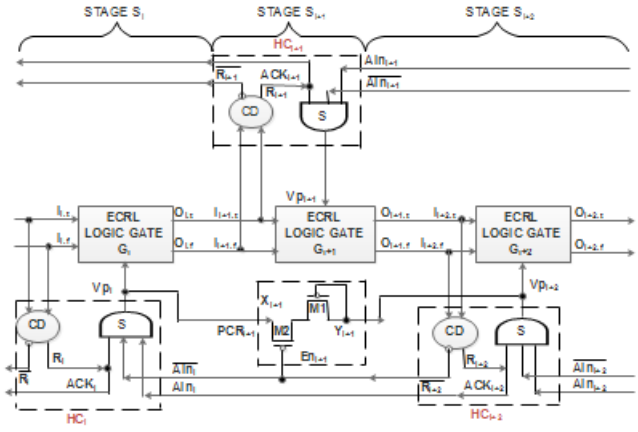
bundled data pipeline is furnished with both a header and footer sleep transistor. At the point when the latch controller in a pipeline stage recognizes valid input data, it assimilates the data in the data latch and turns on the sleep transistor of the related combinational block, so that the combinational block can wake up and process the input data to yield the output data. At the point when the output data is obtained by the successive pipeline stage, an acknowledgement signal is sent again to this stage, and the latch controller can turn off the sleep transistor of the related combinational block to lessen leakage dissipation. However, this technique has the accompanying inconveniences.

In this report, we propose a novel low power logic family, called asynchronous fine-grain power gated logic (AFPL). The AFPL-PCR implementation has the advantage of lower power dissipation, it suffers the problem of a lower maximum sustainable throughput rate. The Sleepy Stack approach gives improved results in terms of static power [3]. This report is sorted out as follows. In Section B, we exhibit the structure of the AFPL pipeline, and depict the logic gates and the handshake controllers utilized as a part of the AFPL pipeline. Section C portrays the PCR mechanism and the Sleepy Stack Sutherland, C-component. Section D shows the simulation results. And lastly, conclusions are given in Section E.

2. AFPL

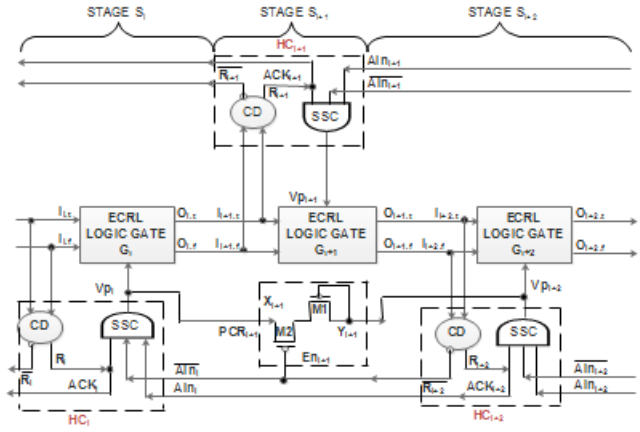
2.1 Overview

In this area, the proposed AFPL is exhibited. Fig.1 demonstrates the structure of AFPL pipeline.



(a)

In AFPL –PCR [see Fig. 1 (a)], a pipeline stage, signified by Si, involves an efficient charge recovery logic [13] (ECRL) entryway Gi, which executes the logic function of the stage and a handshake controller HCi, which manages handshaking with the neighboring stages and gives power to ECRL Logic Gate, Gi.



(b)

Fig. 1. AFPL Pipelines. (a)AFPL-PCR with Sutherland C. (b) AFPL-PCR with Sleepy Stack Sutherland C.

A pipeline stage in an AFPL-PCR is indicated by Si which has an extra unit, the PCR unit PCRi+1, which controls charge value between pipeline stages Si and Si+2. The AFPL-PCR with Sleepy Stack Sutherland C-component [see Fig. 1 (b)], which is utilized as an intend to decrease the input power to the ECRL gate, Gi. It is

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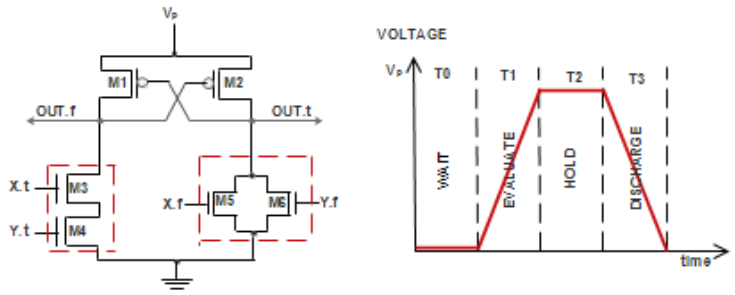
perceived that the synchronization between modules in an asynchronous framework is not accomplished by a global clock, yet rather by nearby handshake Signal, request, and recognize.

2.2 ECRL Logic Gate

An ERCL entryway is utilized to perform the logic functions of AFPL circuit [13]. Fig.2 (a) demonstrates the structure of an ECRL AND/NAND gate.



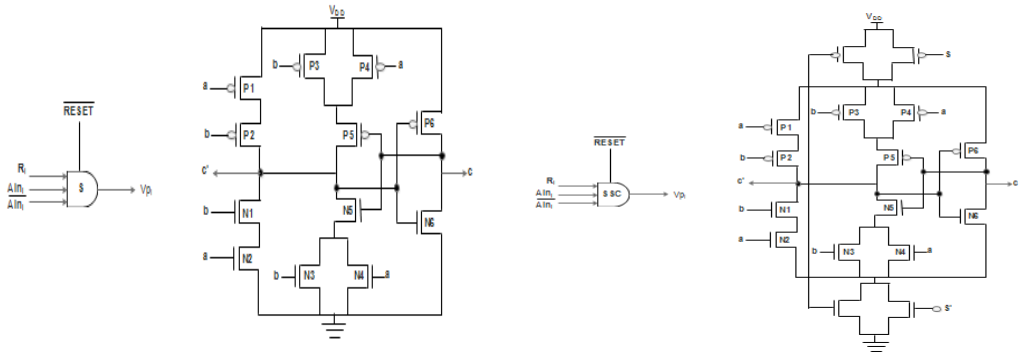
(a) (b)

Fig. 2. ECRL logic. (a) ECRL AND/NAND gate (b)Operation phases for ECRL

ECRL receives dual rail data encoding; that is, each input data into an ECRL gate processes both logic part and its complement. As demonstrated in Fig.2 (a), an ECRL entryway procures power from the power node indicated by, Vp. This power node Vpi is connected with the output of the handshake controller HCi, in an AFPL-PCR. That is, the ECRL gates in the AFPL pipeline obtain power from the handshake controllers rather from a routine altered DC power supply.The operation cycle of an ECRL gate involves four stages,wait,evaluate, hold and discharge. The current operation period of an ECRL gate Gi is detected by the voltage of the associated power node Vpi. Fig.2 (b) demonstrates the voltage waveform of the power node Vpi. In wait phase, the power node Vpi is kept at 0V, and entryway Gi can't draw any current from Vpi. In this way, the comparing gate yields out.t and out.f are both kept low (i.e., void tokens) regardless of the current data values. In the evaluate phase the voltage Vpi increase from 0V to VDD, and gate Gi draws current from Vpi and start to evaluate the output. Whereas in the hold stage, the voltage of Vp stags at VDD, and outputs out. t and out. f stays substantial for the whole hold stage, regardless of the fact that the data get to be void. During the discharge phase, the voltage Vp inclines down from VDD to 0V, the charge on the output node drops down back to the power node Vpi, and the outputs get to be vacant.

2.3 Handshake Controllers:

The handshake controller HCi in stage Si in n AFPL-PCR, performs the accompanying tasks:1)Determining the validity of the inputs to the ECRL logic entryways in stage Si; 2)Offering power to the ECRL logic entryways in stage Si; 3)Determining whether the yield of stage Si has been obtained by the downstream stage Si+2; and 4)Acknowledging the upstream stage Si-2 when Si-2 can uproot its output. As indicated in Fig., a handshake controller is consists of Completion Detector (CD) and a Sutherland component, the CD in HCi is utilized to recognize whether the input to stage Si is a valid code word or void code word. The output of the CD travels from low to high when the data to stage Si turns into a valid code word, and move from high to low when the data to the stage Si turns into an empty code word.



(a) (b)

Fig.3 Structure of the C-elements used in AFPL. (a) Sutherland C element (b) Sleepy Stack Sutherland C element

The structure of the Sutherland component is demonstrated in Fig.3(a) The Sutherland component in HCi has three inputs, Ri , Aini , and Ainibar ,the recent two of which are complement. Ri is the request signal from the CD in HCi . Aini and Aini are the acknowledge signals from HCi+2. After reset, Ri = 0, Aini = 0, and Ainibar =

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1. The transition of Ri and Aini include the accompanying four events. 1) Event Req↑: Ri travels from LOW to HIGH. This event happens when a valid token reaches at stage Si.2) Event Ack↑: Aini travels from LOW to HIGH and Ainibar travels from HIGH to LOW. This events happens when the valid token of stage Si has been gotten by stage Si+2. 3) Event Req↓: Ri travels from HIGH to LOW. This events happens when an unfilled token reaches at stage Si . 4) Event Ack↓: Aini travels from HIGH to LOW and Ainibar travels from LOW to HIGH. This event happens when the vacant token of the stage, has been gotten by stage Si+2.Events ack↑ may happen before or after event req↓ does. The sending of a valid token causes a pipeline stage to evaluate, the sending of an empty token cause a pipeline stage to discharge.

3. PCR MECHANISM AND ENHANCED SUTHERLAND C ELEMENT

Fig.4 shows the 3 stage pipeline AFPL-PCR with Sleepy Stack Sutherland C.A more detailed diagram of 6 stage AFPL-PCR with Sleepy Stack Sutherland C is shown in fig. First, the AFPL-PCR embraces the PCR unit PCRi+1 to control the charge reuse between pipeline stage Si and Si+2. Next, the handshake controller HCi in AFPL-PCR embraces an upgraded Sutherland C called Sleepy Stack Sutherland C element shown in fig., to control the power node of Vpi of the associated ECRL entryways. This Sleepy Stack Sutherland C element provides than an ECRL gate can achieve early discharging if their outputs are no longer needed without waiting for the next empty token to receive at this stage. Gate Gi can enter into sleep mode early with suppressed leakage by introducing Sleepy Stack technique into the Sutherland Element.

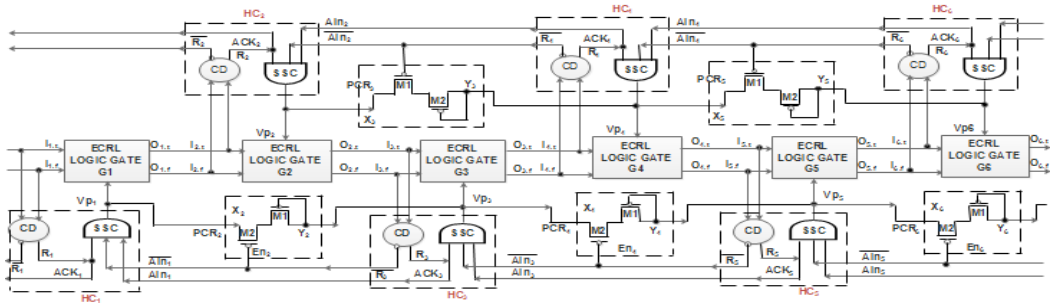

Fig. 4. AFPL-PCR with Sleepy Stack Sutherland C pipeline in six stages.

The benefits of Combining Stacked sleep transistors are 1) the magnitude of power supply fluctuations sleep mode during mode transitions will be reduced because the transitions are gradual. 2) While conventional power gating uses a high- threshold device as a sleep transistor to minimize leakage, a stacked sleep structure can achieve the same effect with a normal threshold device.

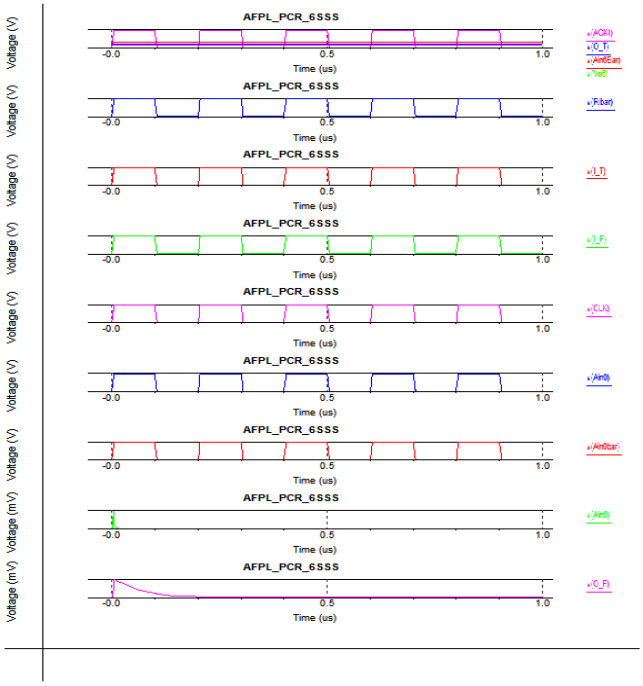

Fig.5Simulation Waveforms of AFPL-PCR with SSC element in six stage pipeline

The operation of AFPL-PCR with Sleepy Stack Sutherland C is like that of AFPL-PCR Sutherland C, aside from that AFPL-PCR with Sleepy Stack Sutherland C adventures early releasing to further lessen energy dissipation. The operation of the Sleepy Stack Sutherland C is like that of Sutherland C component, from the

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operation of the circuit, we conclude that N1, N2 and N6 are the principle pull down transistor, which add to output switching, they are of size W. While N3, N4 and N5 just give the necessary feedback to hold the state of the output when the values of the inputs don't match, thus they are made as little as could be expected under the circumstances to decrease their loading effect. Case in point, let us assume the kth valid token Tvk has arrived at, the input of Si+2 indicated in Fig.1(b). The entry of Tvk at Si+2 causes the going with activities. 1) Aini (i.e.Ri+2) getting to be high causes transistor P5 & P6 in the Sutherland element of the HCi to turn off. Power VDD is cut off from power load Vpi, and ECRL gateGi starts to discharge.2) Eni+1(i.e.Ri+2 bar) getting to be low causes transistor M1 in PCRi+1 to turn ON. On account of charge offering part of the charge on the output nodes of gate Gi streams to a power node Vpi+2 through Vpi and PCRi+1, bringing on entryway Gi+2 to enter the evaluate stage. The charge offering between power nodes Vpi and Vpi+2 can happen just when the voltage of Vpi is higher than that of Vpi+2 plus |Vtp| and the switch transistor M1 in that of Vpi+2 in addition to |Vtp| and the switch transistor M1 in PCRi+1 is turned on. 3) Ri+2 getting to be high causes a power gating transistor N5 & N6 in the Sutherland C component of HCi+2 to turn on. Power rail Vdd begins offering Power to ECRL entryway Gi+2 with the goal that ECRL gate Gi+2 can finish its evaluation.

TABLE I – PERFORMANCE COMPARISON OF VARIOUS PIPELINE CIRCUITS

MODULES	AVERAGE POWER CONSUMED	DELAY IN SEC (OVERHEAD)
3 Stage AFPL-PCR C*Element	11.45	1.25
3 Stage AFPL-PCR S Element	0.624	1.83
3 Stage AFPL-PCR SSC Element	0.373	1.90
6 Stage AFPL-PCR C*Element	3.86	2.12
6 Stage AFPL-PCR S Element	0.145	2.76
6 Stage AFPL-PCR SSC Element	0.040	1.31
6 Stage Kogge Stone adder C*Element	6.53	1.24
6 Stage Kogge Stone adder S Element	1.255	2.54
6 Stage Kogge Stone adder SSC Element	1.235	1.93

Note that Sleepy Stack Sutherland is similar to the Sutherland C element, but the pull up network and pull down network is added in the Sutherland C element. The sleepy stack approach combines the sleep and stack approaches. The sleepy stack technique divide the PMOS and NMOS sleep transistor with same width, into two half size of original single transistor, we add sleep transistor parallel to the two stack transistor of pull up and pull down network [1]. Parallel connection sleep transistor turn ON by providing feedback approach during active mode, all the PMOS and NMOS sleep transistor turn ON, hence resistance of the circuit mitigate. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces the resistance of the path, so the delay is decreased during active mode [18]. During sleep mode, sleep transistor are turned off and stacked transistor suppress the leakage current and maintain exact logic of the circuit. Thus by introducing Sleepy Stack Technique into Sutherland C element, a ultra-low leakage power consumption during stand standby mode is obtained and increase the performance of the circuit by maintaining exact.

4. SIMULATION RESULTS

To assess the viability of the proposed AFPL, we have utilized four logic styles—static CMOS logic, asynchronous PS0 pipeline, AFPL w/o PCR, and AFPL-PCR—to actualize an eight-bit six-stage pipelined Kogge–Stone adder for execution examination using Tanner tool.Table I gives a power dissipation correlation of four logic styles— AFPL – PCR with S element, AFPL-PCR Sleepy stack Sutherland C element —executing an eight-bit Six-stage Kogge– Stone adder with an info information rate running from 30 to 900 MHz.

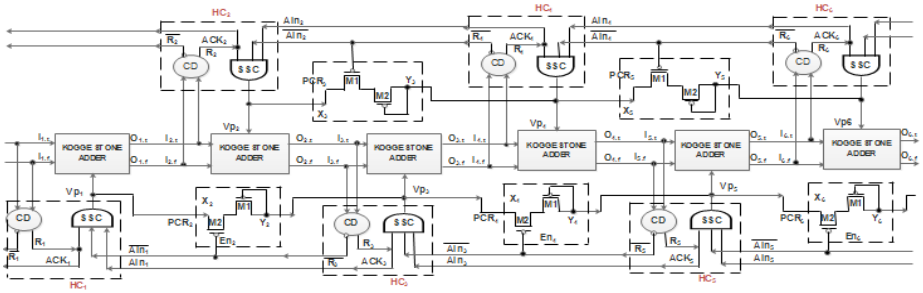

Fig. 6.Kogge Stone Adder with Sleepy stack Sutherland C pipeline with six stages

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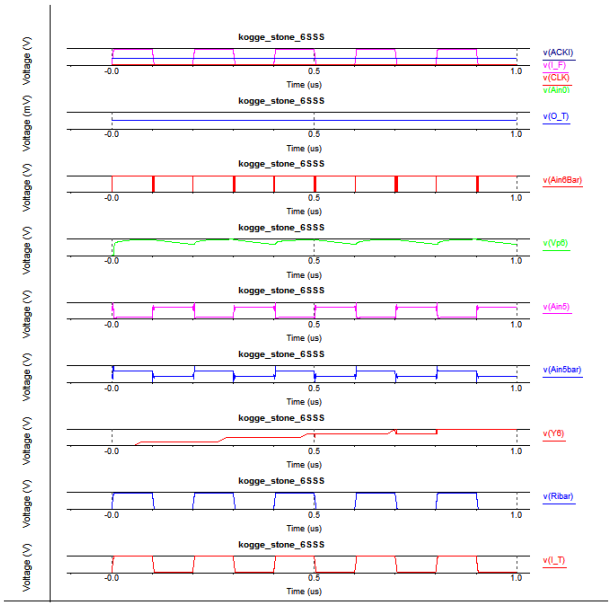

Fig.7Simulation Waveforms of Kogge Stone Adder with SSC element in six stage pipeline

CONCLUSION

This paper has proposed the AFPL-PCR with Sleepy Stack Sutherland C element. The AFPL-PCR pipeline utilizes the improved Sutherland C element called Sleepy Stack Sutherland C element in its handshake controllers such that an ECRL logic entryway in the AFPL-PCR pipeline can enter the sleepy mode right on time to diminish leakage dissipation once its output has been obtained by the downstream pipeline stage. . In contrast the static three stage AFPL – PCR C* element, the three stage AFPL -PCR Sutherland C element usage can decrease power dissipation by 94.5 % and the three stage AFPL-PCR execution with Sleepy Stack Sutherland C element can diminish power dissipation by 40.2 %.In contrast the static six stage AFPL – PCR C* element, the six stage AFPL -PCR Sutherland C element usage can decrease power dissipation by 96.2 % and the six stage AFPL-PCR execution with Sleepy Stack Sutherland C element can diminish power dissipation by 72.4 % in contrast with AFPL-PCR Sutherland C element. Implementing AFPL- PCR in the application kogge stone adder, a six stage kogge stone adder with Sutherland C element reduces leakage power dissipation by 80.7 % in comparison with six stage kogge stone adder with C* element. A six stage kogge stone adder with Sleepy Stack Sutherland C element diminishes leakage power dissipation by 17.5 % in comparison with six stage kogge stone adder with Sutherland C element.

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