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# DESIGN OF LOW POWER MOS SRAM CELL USING 10 TRANSISTORS

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**ABSTRACT**

*Exponential growth in battery powered portable electronic system, demanding high speed, low power SRAM for modern VLSI system. In this paper the conventional 6T SRAM cell operation is discussed. Since several more than 6T SRAM cell are designed to improve the stability and power consumption. Therefore, a new 10T SRAM cell is designed by using two separate word line for read (RWL) and write (WWL) operation to improve the power dissipation, performance and stability. We have assumed one transistor between the two inverters to decrease effective resistance of Pull down network and also two tail transistor for complete charging and discharging of bit lines during write operation. The software that used in designing the new SRAM cell is Microwind DSCH lite3.5 EDA tool.*

***Keywords-*** *CMOS, 6T SRAM, Microwind & DSCH tool, Power consumption.*

## [1] INTRODUCTION

In recent year in the area of low power VLSI circuit design the portability is become very important. In modern world as the technology scaled down due to the introduction of CMOS technology, the memory becomes the basic need of many very large scale integration (VLSI) chips.[1] In today's CMOS technology device has been scale down to achieve higher speed, performance and lower power consumption. As feature size decreases in modern VLSI system, the semiconductor memory become an individual part of system on chip design.

According to ITRS roadmap 90% of chip area will consume by memory. Around 30% of the worldwide semiconductor business is due to semiconductor memory chip. [2] SRAM is widely used as for both on chip cache memory and off chip memory [3]. The main challenge is to increase the performance in term of power and area for SRAM cell with scaling MOS technology and achieving high data stability with reduction in supply voltage.

Reduction in supply voltage is most efficient method for reducing dynamic power dissipation. In this paper with proposed SRAM cell designed with DSCH & microwind 3.5 we use 1V power supply voltage to reduce dynamic power dissipation. Since as the supply voltage decreasing, the threshold voltage of MOS also decreases that will result in increase in sub threshold current or leakage current. So that increased in leakage current due to supply voltage scaling can be controlled by using two tail transistors at the pull down network of the inverters that helps in reducing in leakage current as well as provide proper charging and discharging of bitlines during SRAM read/write operation.

Section I of this paper describe the basic need of memory in current days VLSI circuit design and also explain the modification in proposed SRAM cell to reduce power dissipation and leakage current. Section II explain conventional 6T SRAM cell and Section III explains the proposed SRAM cell, in Section IV simulation result is shown and discussed. In section V we conclude the paper.

## 2. CONVENTIONAL 6T SRAM CELL

**2.1. Functional Approach :-** SRAM is made up of flip flop and it store single bit as voltage. In conventional SRAM cell each bit in an SRAM is store on four transistors that form two cross coupled inverters. As shown in figure (1.1) since the cell consist of latch therefore cell data is kept as long as power is turned on and refresh operation is not required unlike DRAM. DRAM is made up of MOS transistor gate and it stores the bit as a charge. As DRAM have high density and low power consumption and cheaper than SRAM but the main disadvantage is the charge leakage (bit information), therefore store information needs to be refreshed. This is the reason, SRAM is faster than DRAM. SRAM is most commonly used system on chip and is designed to fill two needs ; one is to improve the direct interface with CPU at speed not attainable by DRAM and the other one is to replace DRAM in system that require very low power consumption.

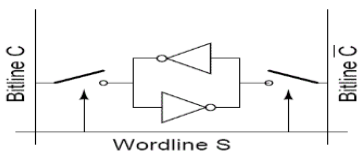


Figure.1.1: SRAM Cell [3]

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**2.2: 6T CMOS SRAM Cell:-** The memory cell consists of simple CMOS inverters connected back to back, and two access transistors. The access transistors are turned on whenever a word line is activated for read or write operation, connecting the cell to the complementary bit line columns. The bitline are connected with two precharge transistors to precharge the bitline before the read operation is performed. The full CMOS SRAM circuit with precharge transistor is shown in figure (1.2)

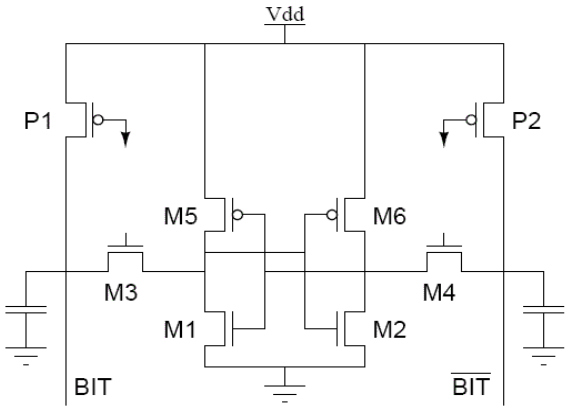


Figure 1.2. SRAM circuit with precharge transistor [4]

**2.3: Operation of SRAM cell: -** As shown in Fig.(1.3) circuit diagram of a conventional 6T SRAM cell has Word line (WL) is used for enabling the access transistors T2 and T5 for write operations. The bit line BL and BL bar line are used to store the data and its compliment.

During operation of SRAM cell the W/L ratio is one of the most important parameter which dictates the data **read** operation should not destroy the stored information in the cell. The cell should allow stored information modification during **write** operation. For proper operation of SRAM, we have to consider the relatively large parasitic column capacitance and column pull-up transistors as shown in Figure (1.2) When none of the word lines is selected, the access transistors M3 and M4 are turned off and the data is retained in all memory cells. The column capacitances are charged by the pull-up transistors P1 and P2. The voltages across the column capacitors reach **Vdd - VT**.

**Writing operation**, for proper writing operation, one bit line is high and the other bit line is low. For writing "0", BL is low and BL bar is high. When the word line (WL) is asserted high, both access transistors T2 and T5 are turned ON and any charge which is stored in the BL goes through T2-T3 path to ground. Due to zero value on Q bar, the transistor T4 is ON and T6 is OFF. So the charge is stored at Q bar line. Similarly in the write "1" operation, BL is high and BL bar is low, due to this T6 is ON and the charge stored on Q bar is discharged through the T5-T6 path and due to this low value on the Q bar , T1 is ON and T3 is OFF, so the charge is stored on the Q.

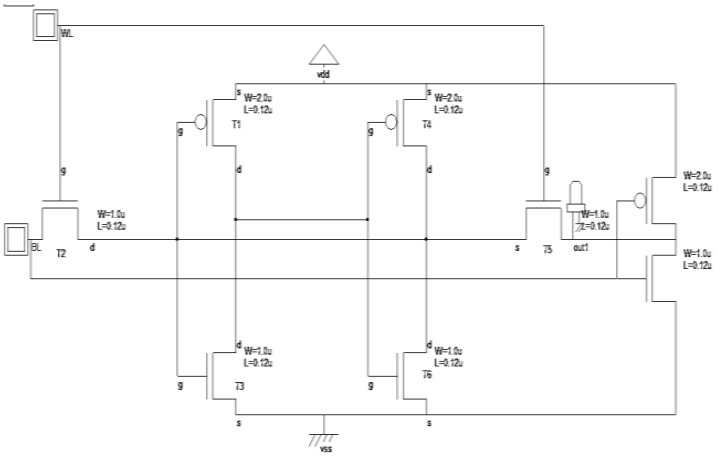


Figure1.3 a conventional SRAM cell [5]

Before the read operation of "1" at Q (for example) begins, BL and BL bar are pre-charged to as high as Vdd. When the WL is selected, the access transistors T2 and T5 are turned ON. Because of the pull-up transistor T1 ON and pull down transistor T3 OFF, voltage of BL will be nearly Vdd. On the other side, current will flow from the pre-charged BL bar to ground, thus discharging BL bar line through T5-T6 path to ground; T4 being OFF. Thus, a differential voltage develops between BL and BL bar lines. This small potential difference between the bit lines is sensed and amplified by the sense amplifier at the data output.

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## 3. PROPOSED SRAM CELL

In order to improve the performance of conventional SRAM cell during normal mode (Read and Write) and standby mode (SRAM contains previously written value) with the reduction in power consumption and leakage current there is one method to make modification in conventional SRAM circuit in such a way that the proposed SRAM circuit help in reducing the power consumption and leakage current and also manages the charging and discharging the bit line during read and write operation.

As discussed by previous researcher Singh et al. in Symmetric and Balanced 11-T SRAM cell [6], the new proposed SRAM cell is designed by using 10 transistors including six transistors similar to conventional SRAM cell. The proposed SRAM cell include two tail transistor at the bottom of the pull down network of latch and both are cross coupled with bitline and bitbar line to control the charging and discharging of bit lines during write operation and also helps in controlling the leakage current in standby mode. The bit line is connected with an inverter to create a complementary input at the bitbar line.

In this new SRAM cell the read operation and write operation is performed by two different word lines WWL and RWL. During write operation RWL is low and WWL is activated similarly during read operation the WWL is low and RWL is high.

There is one another transistor is connected between the two cross coupled inverters that will help in reducing the effective resistance of the pulldown network of inverters and is responsible for read operation by connected the gate of this transistor to the RWL (read word line) signal. Last one transistor also added in new proposed SRAM cell nearly one of the access transistor to create a separate path for read operation of new SRAM cell by connecting RWL signal with gate of this transistor and drain terminal is connected at output of one inverter. The schematic circuit of proposed SRAM is shown in figure (1.4)

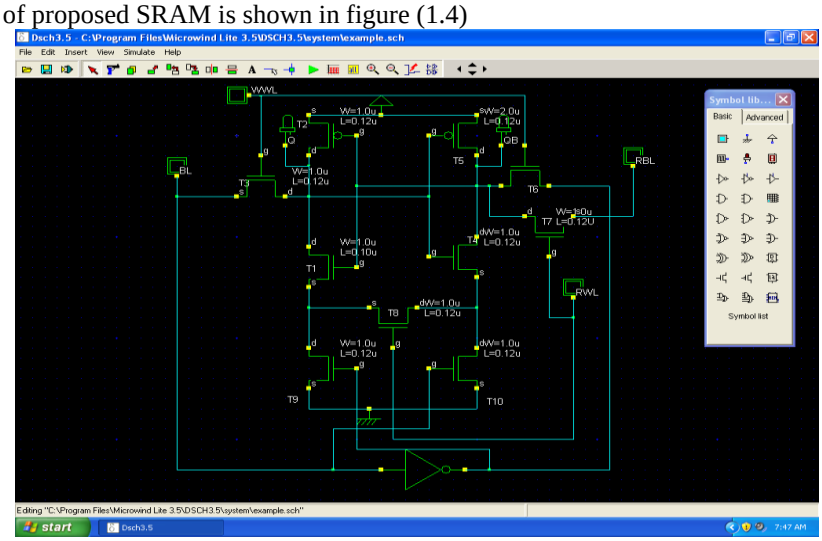


Figure 1.4. Schematic circuit of proposed SRAM

**During write operation** WWL is set to high and RWL is set to low. For performing the writing operation proper values should be asserted to the bitline and bitbar line. The critical path for writing operation of this proposed SRAM cell is shown in figure (1.5). As shown in figure (1.5) by activating the WWL at high and give a high signal to bit line then it sets the bitbar line at its complementary input through an inverter. Since the WWL goes high the two access transistor T3 and T6 is in on position after that when bitline sets to high, one inverter pullup transistor T2 and other inverters pulldown transistor T4 is in on position to write 1 at Q and 0 at QB. There is one of the tail transistor is also on and other one is off for proper bitline charging and discharging, that is voltage swing to reduce dynamic power dissipation. As dynamic power dissipation of CMOS inverter is defined as: [7]

$$P_{dynamic} = \alpha C V_{dd} V_{swing} f$$

Where, α is the switching activity C is the load capacitance capacitance, $V_{dd}$ is the supply voltage, f is known as the clock frequency , and $V_{swing}$ is the switching Voltage.

The dynamic power dissipation is reduced by reducing the switching voltage and supply voltage. [8] In this proposed SRAM cell we use only 1 Volt power supply voltage using DSCH and microwind that result in decrease in power dissipation but at same time due to supply voltage decrease the threshold voltage of MOS also decrease that will result in an increase in leakage current that is controlled by creating a path through one of tail transistor to ground.

Before **the read operation** the bit lines are properly precharged that is the RBL(read bit line ) input and bit bar lines set to high. In case of read operation the WWL set to low and RWL set to high. As the figure (1.6) shows that, to performed read operation first set WWL at low value after that precharge read bit line at high after that as we turn on the RWL the transistors T1, T5, T7, T8 and T9, are on depending on the previously stored data at

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nodes Q and Qb that is either read 0 or 1 can be performed. The critical path for read 1 operation is shown in figure (1.6) in this case one of the two bitlines will be pulled down by the cell and read operation will be performed. The transistors T1, T5 T7, T8, and T9 are being on to provide the read path on Qb node set to and Q node set to 0 in the proposed SRAM cell.

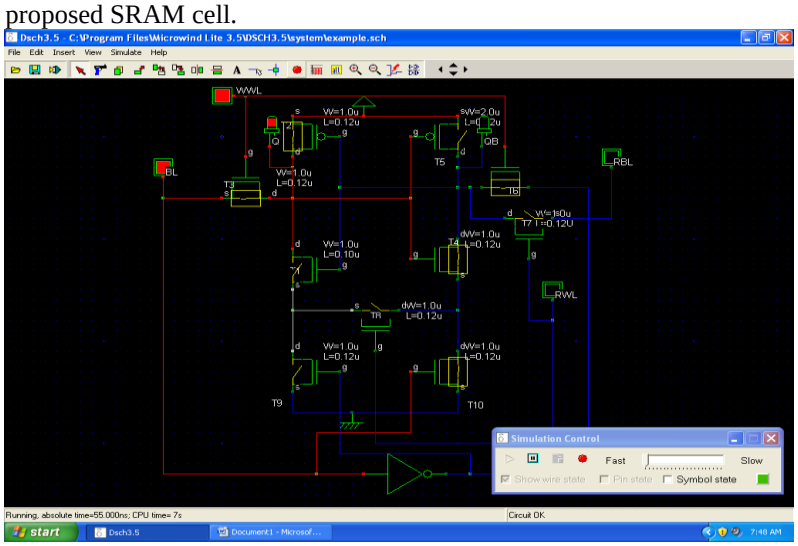


Figure 1.5 Writing path of proposed SRAM cell

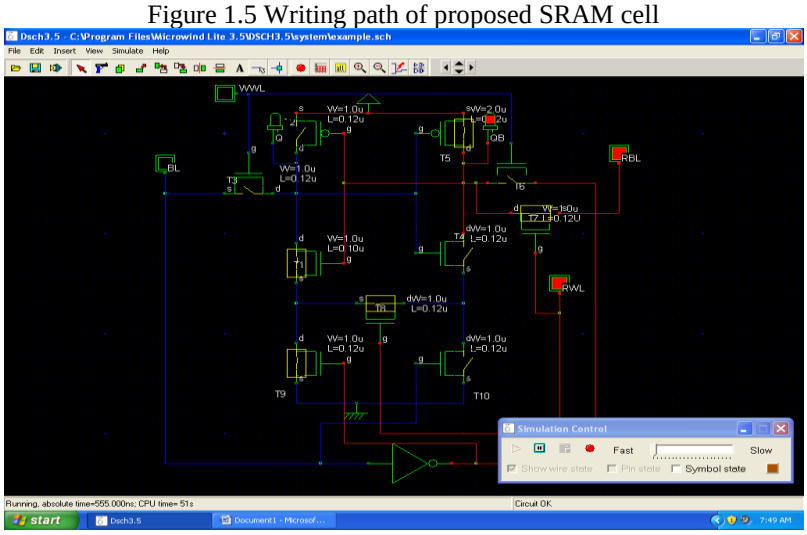


Figure 1.6 critical path of read 1 operation

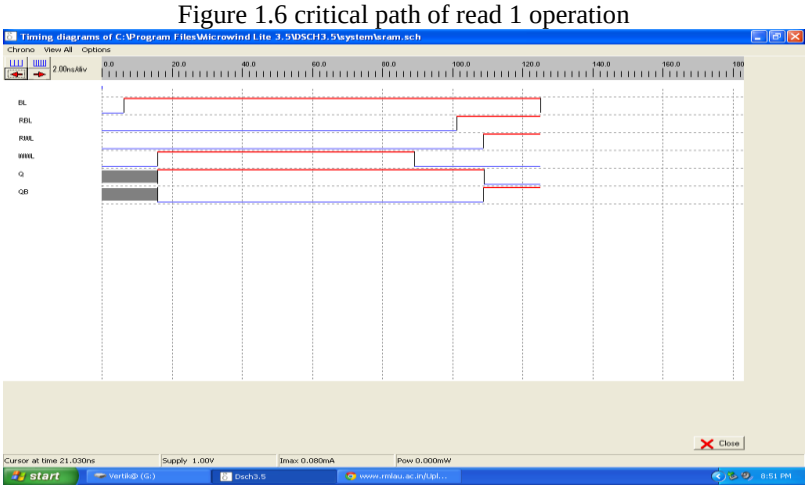


Figure 1.7. Simulation analysis of 10T SRAM cell

## 4. RESULT AND DISCUSSIONS

In this section we have provided the detailed simulation analysis of this proposed SRAM cell by using DSCH and microwind 3.5 lite. This paper is an attempt to design proposed 10T SRAM cell that gives an improved

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performance stability during read and write operation by utilizing the two separate wordlines for read and write operation. It also improves the dynamic power dissipation by controlling the power supply voltage 1 volt used in this proposed SRAM cell and also reduce charging and discharging of bit lines by adding two tail transistors in proposed cell. The detailed simulation analysis result is shown in figure (1.7)
From the simulation analysis result shown in figure (1.7), it is clear that during write operation WWL is high and RWL is low. Output Q goes high and QB low the write '1' at Q & '0' at QB is performed. As the WWL goes low and RWL goes high the output changes QB goes high and Q goes low, read '1' operation is performed.

## CONCLUSIONS

In low power high speed VLSI design the dynamic power consumption becomes a very challenging task for SRAM with reduction of supply voltage. This has demanded an efficient SRAM cell design which should have low leakage current and to achieve high data stability. In proposed SRAM cell we use 1V supply voltage to reduce dynamic power consumption. This proposed SRAM cell is designed by two separate wordlines WWL and RWL to implement the read and write assist circuit techniques with high data stability. This proposed SRAM cell can be used to provide low power utilization for many portable devices like laptop, mobile phone and programmable logic devices. The proposed SRAM cell can be further improved in future during its normal mode of operations to become more power saving SRAM cell.

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## REFERENCES

[1] International Technology Roadmap for Semiconductors by Semiconductor Industry Association, http://public.itrs.net, 2007.
[2] Abhishek kumar, "SRAM Cell Design with minimum number of transistor" Proceeding of 2014 RAECS UIET Pnjab University Chandigarh 06-08 March, 2014
[3] Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000 Integrated Circuit Engineering Corporation "Sram Technology" pp. 8.10- 8.
[4] Kang &Leblebigi "CMOS Digital IC Circuit Analysis & Design"- McGraw Hill, 2003
[5] S. Mohan Das, K. S. Kiran Kumar, A.Madhulatha, "A Novel Low Power Energy Efficient SRAM Cell With Reduced Power Consumption using MTCMOS Technique" IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 5, Issue 1, Ver. I (Jan - Feb. 2015), PP 42-49 e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
[6] Singh AK, Prabhu CMR, Pin SW, Hou TC. A Proposed Symmetric and Balanced 11-T SRAM Cell for lower power consumption. TENCON. 2009: 1-4.
[7] Labonnah Farzana Rahman, Mohammad F. B. Amir, Mamun Bin Ibne Reaz,Mohd. Marufuzzaman, Hafizah Husain, "Advances on Low Power Designs for SRAM Cell" TELKOMNIKA Indonesian Journal of Electrical Engineering Vol. 12, No. 8, August 2014, pp. 6063 ~ 6082
[8] Upadhaya P, Mehra MR, Thakur N "Low Power Design of an SRAM cell for portable devices" International conference or computer & Communication Technology (ICCCT'10) 2009: 255-259
[9] Abhishek Agal, Pardeep, Bal Krishan. 6T SRAM cell: Design and Analysis. IJERA; Volume 4, Issue 3(Version 1); March 2014; pp 574-577.
[10] Sapna singh, Neha Arora, Meenkshi Suthar, Neha Gupta. Performance evaluation of different SRAM cell structures at different technologies. International Journal of VLSI design& communication systems (VLSICS); vol.3, No.1; February 2012.
[11]Uppunuthula Pavani Srinivas Kuntamalla " A Low Power CMOS voltage mode SRAM cell for high speed VLSI Design" International Journal of Advances in Applied Science and Engineering (IJAEAS) ISSN (P): 2348-1811; ISSN (E): 2348-182X Vol-1, Iss.-4, SEPTEMBER 2014, 87-90 © IIST
[12] Microwind and Dsch v3.0 – Lite User's Manual –Etienne Sicard.
[13] N. Yoshinobu, H. Masahi, K. Takayuki, K. Itoh. Review and future prospects of low-voltage RAM circuits. IBM journal of research and development; vol. 47, No. 5/6; pp.525-552; 2003
[14] L.Chang, et al. "Stable SRAM Cell Design for the 32 nm Node and Beyond", VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on, 14-16 June 2005 Page(s):128 -129
[15] R. Aly, M. Faisal and A. Bayoumi. Novel 7T SRAM Cell For Low Power Cache Design. IEEE SoC Conf., 2005.