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DESIGN OF DC-DC CONVERTER FOR SOLAR APPLICATION

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ABSTRACT

Electronic applications today are portable and wireless, rechargeable batteries are mandatory to provide the required energy. Although prone to innovation and improvement, the battery voltage does not scale with the CMOS technology power supply voltages. Obviously, this is due to their physical and chemical constraints. A DC-DC converter is a device that converts a Direct-Current (DC) voltage Vin into a lower or higher DC voltage Vout, if Vout > Vin then it is called as step-up converter or boost converter and for Vin> Vout it is said as step up down converter or buck converter. Moreover a DC-DC converter is considered as to be a impedance transformer. In this DC-DC boost converter is designed for solar application using CMOS 0.18µm technology with 1MHz switching frequency. There are two main units responsible for operations of the converter namely control unit and power unit. Control unit is realized using pulse width modulation control system which involves design of operational amplifier, comparator and provides necessary path for charging and discharging. Power stage involves mosfet's used for providing necessary voltage and current at the output. This paper emphasizes on the design of both boost and buck converter to switch the voltage from one level to another level, the input power is derived from a photovoltaic cell which is fed to the converter. The converter is simulated using LT-spice.

Keywords: *CMOS, boost converter, pulse width modulation.*

[1] INTRODUCTION

In the modern day we can see that electronic devices tend to be portable and wireless in application, and the growing use of these devices implies that there is a need for more energy. The high demand for energy and depleting fossil reserves or non-conventional resources is a point of concern. This paper aims in providing a solution to harness the renewable source of energy. There a different source of renewable source of energy like wind, hydro-electricity, geo-thermal, nuclear energy etc, but in this paper solar energy is taken as it is abundantly available everywhere and implementation is of less cost compared to other form of generating energy.

This paper presents design of DC-DC converter for low power application. The design of DC-DC converter becomes important as portable electronic devices are in great use, so power management becomes very important in semiconductor industry. The power management in semiconductor is performed using either buck or boost converter and various voltages are generated for different application. This paper emphasizes on design of boost converter and buck converter.

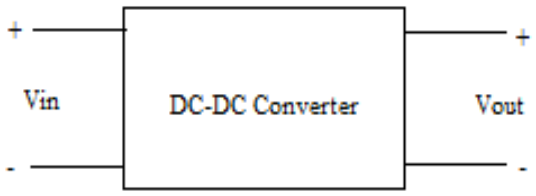

Figure 1: Black Box of DC-DC Converter

The converter usually composed of a power stages in which provide the necessary potential difference and power at the output and the control unit which is the heart of the circuit. Selection of proper values of inductor and capacitor, widths of mosfet, operational amplifier, comparator and, sawtooth wave oscillator play pivot role in the working and performance of the boost converter. Voltage mode control circuit is used against current mode control, as current mode control involves lot of complexities in realizing the circuit. CMOS 0.18µm technology is used in designing the control circuit to achieve low noise and fast transient signal in the PWM signal. The control unit designed in this paper is same for buck and boost conveter. In this both buck and boost converter were operated in continuous conduction mode (CCM). In CCM current across the inductor in not zero at any given time.

The schematic of the boost converter is presented in figure 2. Figure 2 depicts a converter with a power stage and control stage. Transistor MN1 and MP1 form the power stage. Power stage consists of inductor (L) and capacitor (C) of 400nH and 2.5µF. Control unit is designed using same 0.18µm CMOS technology which consists of operational amplifier and comparator. The voltage to error amplifier is referred through the resistive network of R_1 and R_2.

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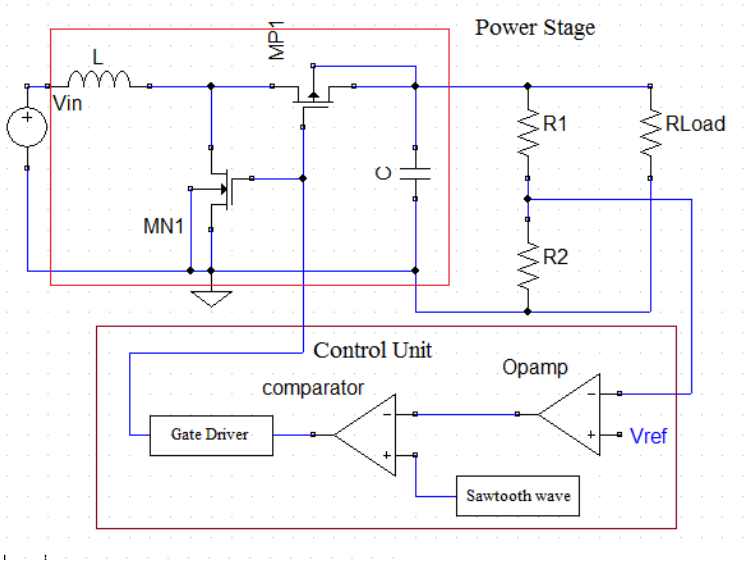

Figure 2: Schematic of DC-DC Boost Converter

The schematic of buck converter is shown in figure 3. Buck converter finds their high use in low power application as a rectifier. In this design, MOSFET MN1 is the main MOS responsible for the required voltage and power at the output. MOS MP1 is used in the place of the traditional diode, this helps in preventing greater loss, low resistance path and, faster transients of the circuit. The output set of capacitor and inductor together form a filter, which filter out AC component and provide only DC component at the output. In this main MOS MN1 is subjected to voltage stress. The output inductor is selected in such a way that current does not change with time and capacitor to see that output voltage consist of fewer ripples relatively. The values of output capacitance and inductor are 16µF and 16µH respectively.

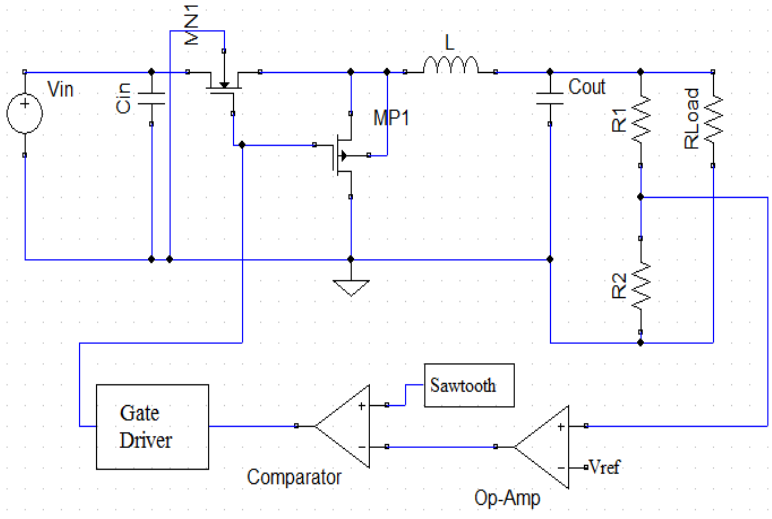

Figure 3: Schematic of Buck Converter

2. CONTROL UNIT

2.1ERROR AMPLIFIER

The error amplifier is realized using operational amplifier, which is also a CMOS operational amplifier with fast transient response and with low power consumption, which indirectly improves the efficiency of the converter. Operational amplifier shown in figure 2 consists of current mirror, input differential stage and a common source stage. A compensator is also included to improve the stability of the frequency response of amplifier and to obtain fast transient. When compensation is accounted the feedback network must be taken into account as stability and phase margin depend upon the loop gain. Figure 3 is a undriven op-amp fro both inverting and non-inverting configuration. Op-amp has relatively high input impedance. The loop gain is given by equation 1.

$$L(s) = A_v(S)\frac{Z_1}{Z_1 + Z_2} \quad \text{.....1}$$

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There are several ways to factor out L(S), the best way is to factor into A(s) and β, where $\beta = Z_1/(Z_1 + Z_2)$ and adding to it β is constant upto loops unity frequency β = 1, hence L(S) = $A_V(S)$. The capacitor C_C, controls the dominant first pole and loop's unity gain frequency ω_T and is given by equation 2.

$$\omega_T = L_0\omega_{p1} = \frac{\beta g_{m1}}{C_c} \quad \text{.....2}$$

Lead compensation is accomplished using R_c which gives in third order denominator resulting in a zero, zero is given by ω_z and equation 3.

$$\omega_z = \frac{-1}{C_C(1/g_{m7} - R_c)} \quad \text{.....3}$$

Zero in the right half plane can be eliminated by choosing R_C with higher value and which helps in shifting the zero to left half plane. Therefore

$$R_c = \frac{1}{g_{m7}}\left(1 + \frac{C_1 + C_2}{C_c}\right) \quad \text{.....4}$$

$$\omega_z = 1.7\omega_T \quad \text{.....5}$$

$$R_c \cong \frac{1}{1.7\beta g_{m1}} \quad \text{.....6}$$

R_c may be replaced by a mos transistor, which is operating where V_{DS}=0, so there is no bias current flowing, which can be given by equation 7.

$$R_c = r_{dsq} = \frac{1}{\mu_n C_{ox}\frac{W}{L}V_{eff}} \quad \text{.....7}$$

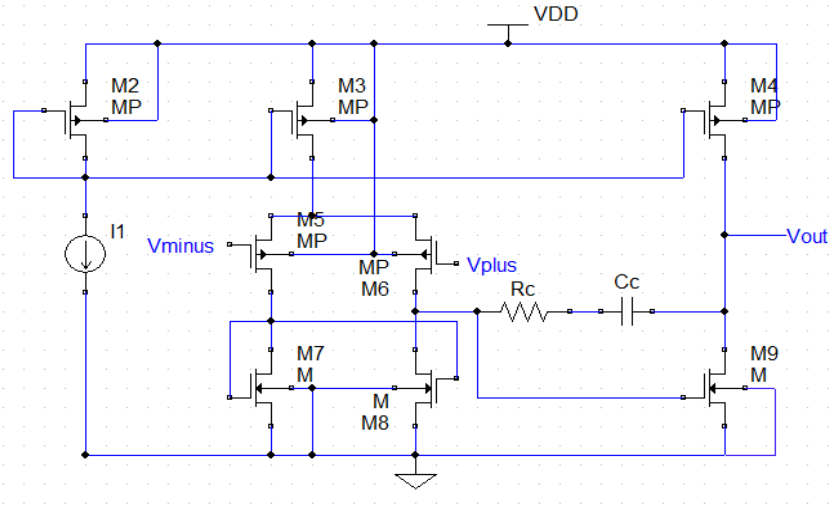

Figure 4: Schematic of Op-amp with compensator

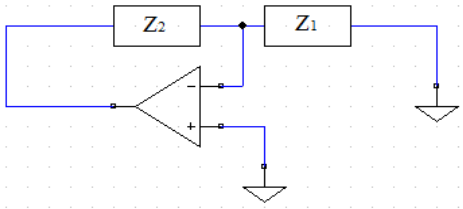

Figure 5: Undriven Op-amp Network with general feedback

2.2 OTHER CIRCUITS

The comparator used in the pulse width modulator is schematic used in figure 4. The comparator is same like the operational amplifier used in the error amplifier with input differential stage, bias circuitry, common source

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follower and an inverter at the output to switch to any one of the stable state. In this op-amp has a gain of 1043 v/v so a small differential input is amplified largely so with the help of an inverter modulating its aspect ratio we can swing to anyone its stable state. In this if $V \leq V_{ref}$ then output is logic high or logic '1' and for the remaining condition it is logic low or logic '0'. In this comparator the inverting terminal is fed by output of error amplifier and to the non-inverting terminal sawtooth wave generator is connected. The difference of the two decides the charging and discharging time of the boost converter. The output of the comparator is connected to the gate driver.

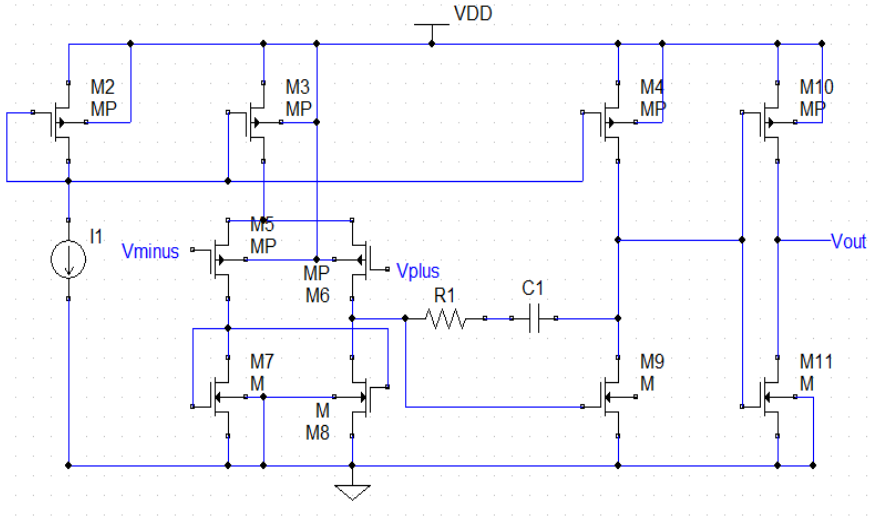

Figure 6: Schematic of a Comparator

The gate driver for this converter is a series of two inverter in cascaded from and the two inverter bear different aspect ratio so that rail to rail swing of 0 to V_{DD} is achieved. This gate driver will finally drive the mos transistor of power stage. The gate driver also ensures that control unit is not loaded.

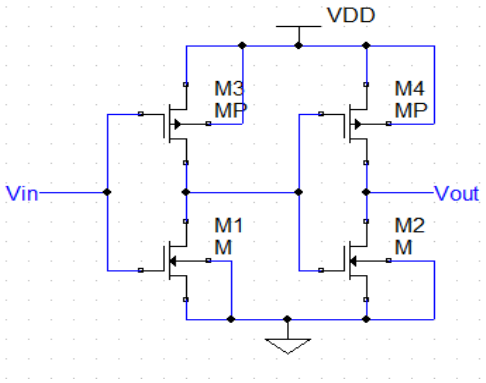

Figure 7: Gate Driver

3. RESULTS

The DC-DC boost converter is designed to work at 1MHz of switching frequency. Pulse wave is used to determine switching period of individual transistor .Figure 8 shows the pulse waveform at the output of the control unit. To get a continuous pulse at the output of the control unit, the output of the error amplifier should never be equal to zero because if it is zero then the inductor will be in either charging or discharging phase only so resulting in some arbiter output which is not faithful for the converter.

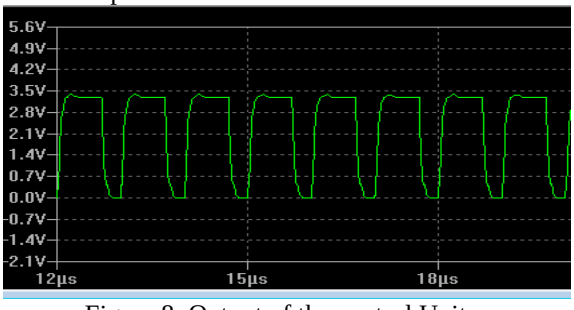

Figure 8: Output of the control Unit

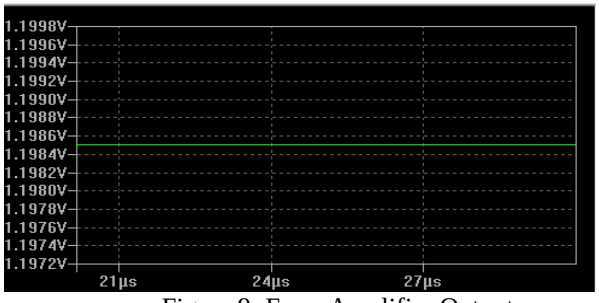

Figure 9: Error Amplifier Output

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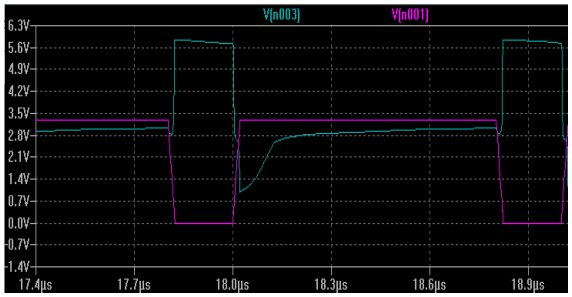
The input to the error amplifier is feedback through the resistive network R_1 and R_2 and reference voltage. The difference is amplified and is given as input to the comparator. The output of error amplifier is never equal to zero. Its output is shown in figure 9.

The current through the inductor and the inductor voltage measured after the inductor, 3.3V potential difference is applied to input to the inductor with inductor value of 400nH and output capacitor of 2.5µH.



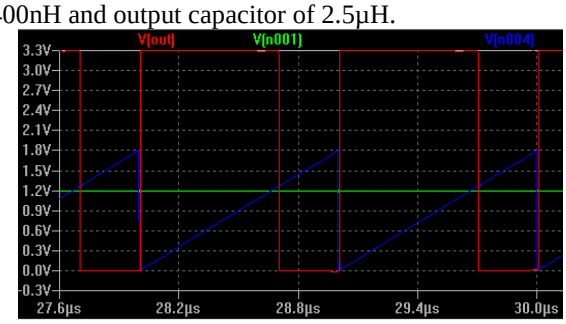
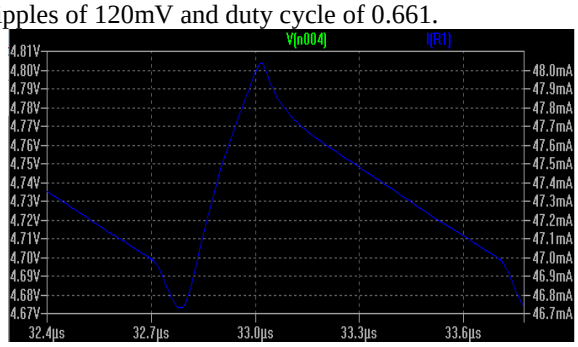


Figure 10: Inductor Voltage after Inductor block

Figure 11: Output of sawtooth wave generator, error amplifier and, gate driver

Figure 11 shows the important control system output of the error amplifier, sawtooth wave generator, and output of gate driver. The switching of off to on or vice-versa can be observed from the following figure 11. Figure 12 shows the simulation of the converter with maximum output voltage of 4.8v and current of 48mA with output ripples of 120mV and duty cycle of 0.661.



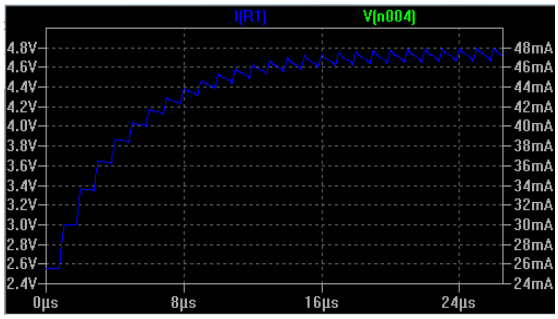


Figure 12: Output of DC-DC Converter Voltage and Current

The performance of the designed DC-DC boost converter is shown below in table 1.

Table 1: Performance of Boost Converter

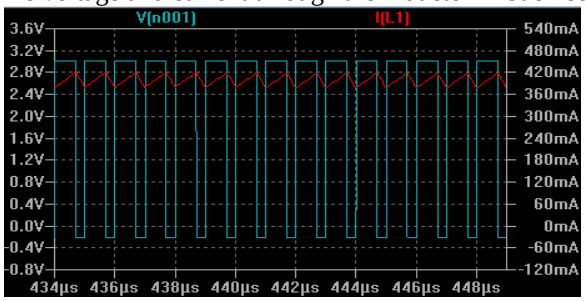
Technology	0.18µ CMOS
Input Voltage (Vin)	3.3V
Output Voltage (Vout)	3.4V – 4.8V
Load Current	33mA – 94mA
Ripple Voltage	120mV

The DC-DC buck converter was designed to work at 1MHz switching frequency. The same control unit design for boost converter was used here. Table 2 shows the performance characteristics of buck converter.

Table 2: Performances of Buck Converter

Technology	0.18µ CMOS
Input Voltage	12V
Output Voltage	1.5V – 2.1V
Load Current	202mA – 1A

The voltage and current through the inductor in buck converter is shown in figure 13.



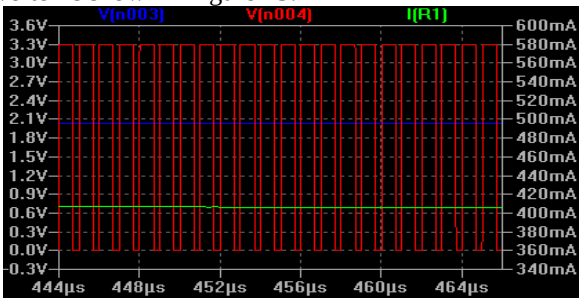


Figure 13: Voltage and Current through Inductor in Buck Converter

Figure 14: Voltage and Current at output of Buck Converter

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Voltage and Current at output of buck converter. From this figure we can say that converter is in continuous conduction mode.

CONCLUSION

In this paper DC-DC converter for low power application was designed and simulated. 0.18µ CMOS technology was used in designing the mosfet of Power Stage and Control unit of the converters. The performance for both the converter in Table 1 and Table 2 was met.

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