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An Area-Efficient Carry Select Adder Designed by Using Transmission Gate

JISMI.T.A[1], NITHIN JOSE K[2]
[1]Department of E.C.E, College of Engineering Trikaripur, Kasaragod, Kerala.
[2] Department of E.C.E, Cochin College of Engineering and Technology, kerala.
[1]jismita510@gmail.com,[2]nithinjosee@gmail.com

ABSTRACT

Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification the transistor count is again reduced by using common Boolean logic term, the newly proposed architecture has been compared with the regular CSLA architecture. The proposed designs have reduced area and power as compared with the regular CSLA with only a slight increase in the delay. The results analysis shows that the proposed CSLA structures are better than the regular CSLA.

Keywords: Carry Select Adder, Power consumption, Boolean logic, Transmission gate

[1] INTRODUCTION

In conventional carry select adder shown in fig.1 contain duplicated full adders, so the transistor count and power consumption is high. To reduce the power consumption and area required by the CSLA, simplify the duplicated full adders by sharing common Boolean logic term as shown in fig.2. In this according to the 'carry in' signal multiplexer selects the correct output.

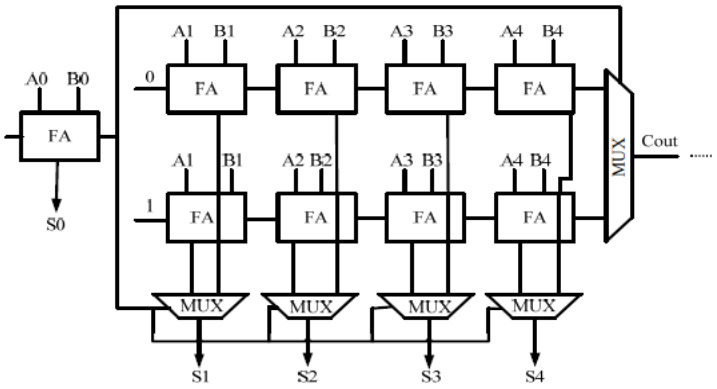

Fig.1. 5-bit carry select adder

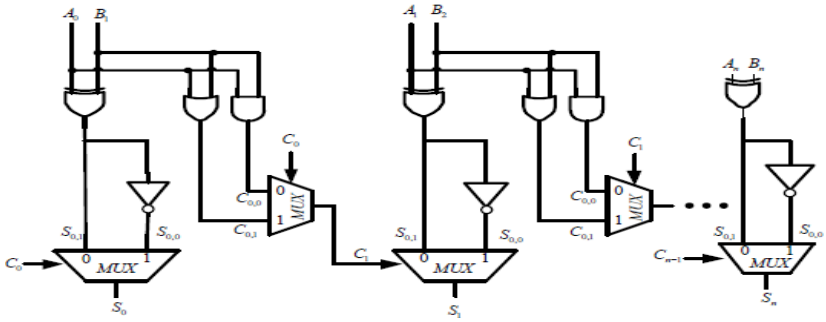

Fig.2. The area-efficient carry select adder

This paper explains the already existing carry select adder techniques in part [**2**] as a review. Then in part [**3**] it explains the proposed work and comparison table. In part [**4**] the experimental results and analysis of the work will be discussed. Final part [**6**] will be the concluding section of the paper.

[2]. REVIEW ON CARRY SELECT ADDER

Deepthi Obul Reddy, P.Ramesh Yadav in 2012[7] proposed a Carry Select Adder with Low Power and Area Efficiency. In performing fast arithmetic functions, Carry select adder (CSLA) is one of used in many data processing processors to perform fast arithmetic functions. CSLA (SQRT CSLA) architecture have been

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developed and compared with the regular SQRT CSLA architecture. The proposed design has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay. This work evaluates the performance of the proposed designs in terms of delay, area, power. The result analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA.

K.Saranya in 2013 proposed [8] a low power and area efficient carry select adder . This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. The proposed design has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay.

Garima Singh in 2014[9] proposed a Design of Low Area and Low Power Modified 32-BIT Square Root Carry. In digital circuitry, a compact and fast adder is required to carry out computations in large chips. Carry Select Adder (CSLA) is one of the fast adders used in many data-processing processors to perform fast arithmetic functions. Although carry select adder is slower than carry look-ahead adder but area is lesser. From the structure of the CSLA, there is scope for reducing the area and power consumption in the CSLA. The thesis uses a simple and efficient gate -level modification to significantly reduce the area and power of the CSLA. Based on this modification 32-bit square-root CSLA (SQRT CSLA) architecture has been developed and compared with the 32-bit conventional SQRT CSLA architecture.The modification is the use of Binary-To-Excess-1Converter logic instead of the chain of full adder when carry is 1.

I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng in 2012 proposed[3] an Area-Efficient Carry Select Adder Design by Sharing the Common Boolean Logic Term. This paper deals with an area-efficient carry select adder by sharing the common Boolean logic term. After logic simplification and sharing partial circuit, there is of need one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation. Through the multiplexer, we can select the correct output result according to the logic state of carry-in signal. In this paper a new approach taken to deal with carry generation and summation. By using this new approach, it is possible to reduce the gate level and also the power dissipation. But based on this paper it is possible to again reduce the gate level by implementing some modification to this. It provides better results compared to previous method. Modification to the existing carry select adder by sharing common Boolean logic term is done based on this paper.

[3]. PROPOSED METHOD

The existing architecture by sharing common Boolean logic term is again modified to significantly reduce the number of transistors and also power consumption. The modification is done by using transmission gate. That is, in the modified architecture the two input multiplexer is replaced with transmission gate for the sum and carry generation to reduce the power consumption and area. This is shown in fig. 3.

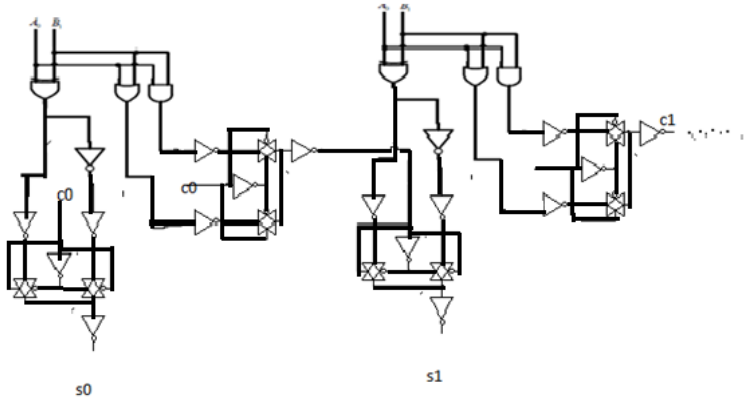

Fig.3. Proposed carry select adder

This system is simulated by using Microwind. Microwind is a friendly educational tool for designing and simulating microelectronic circuits at layout level. The tool features full editing facilities (copy, cut, paste, duplicate, move) various views and an analogue simulator. The simulation output can be viewed as a waveform after the application of input.

[4]. RESULTS AND COMPARISONS

The simulation output waveform views of existing and proposed Carry select adder is given. The proposed Carry select adder code circuit is also simulated and waveform obtained. The existing and proposed circuits are simulated by using the simulation tool "MICROWIND". The performance analysis compares existing and proposed Carry select adder circuit.

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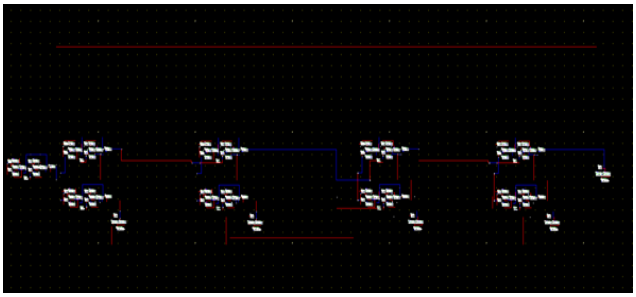

Fig.4. Layout of carry select adder

Fig.4. shows layout design of existing regular 8-bit carry select adder by using Micro wind tool.

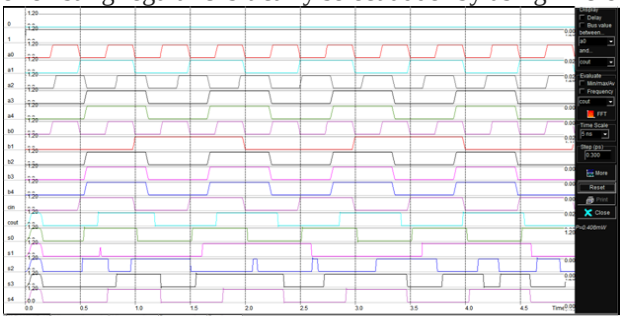

Fig. 5. Simulation output waveform

Fig. 5. shows the simulation output of existing regular 8-bit carry select adder by using Micro wind tool.

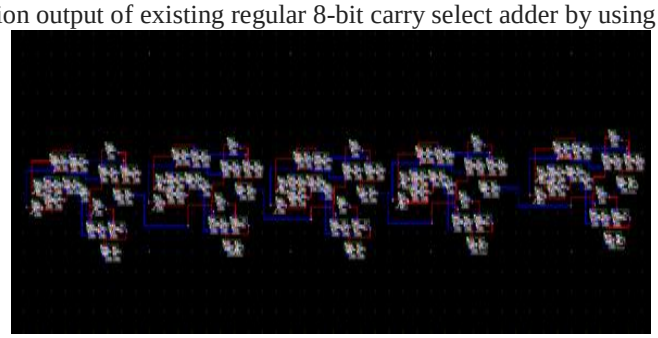

Fig.6. Layout of area efficient carry select adder

Fig. 6. shows the layout design of existing area efficient 8-bit carry select adder by sharing common Boolean logic term .

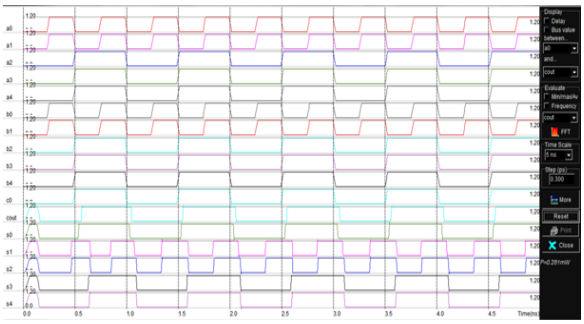

Fig.7..Simulation output

Fig. 7. Shows the simulation output of existing area efficient 8-bit carry select adder by sharing common Boolean logic term

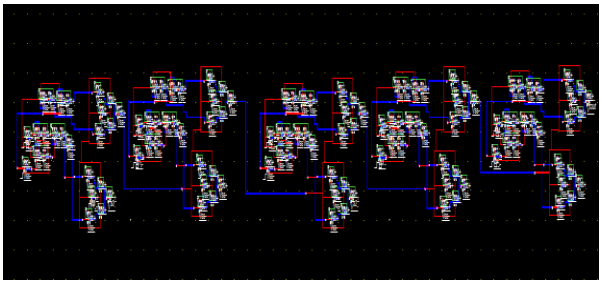

Fig.8. Layout of proposed CSLA

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Fig. 8. shows the layout design of proposed area efficient 8-bit carry select adder by using transmission gate

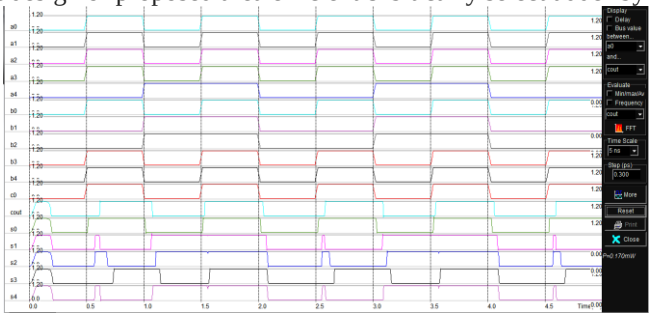

Fig .9.Simulation output of proposed CSLA

Fig. 9. shows the layout design of proposed area efficient 8-bit carry select adder by using transmission gate.

Designed and analyzed an area efficient carry select adder by using microwind software and the power consumptions are noted. Here we observed that the proposed architecture have low power consumption and area compared to existing regularCSLA and carry select adder by sharing common Boolean logic term .This is shown in table .

	NUMBER OF TRANSISTORS	POWER CONSUMPTION(mw)
BASIC CSLA	52	.408
AREA EFFICIENT CSLA BY SHARING COMMON BOOLEAN LOGIC	48	.281
PROPOSED CSLA	40	.170

[5]. CONCLUSIONS

In this paper, the comparisons of existing carry select adders with different architectures have been studied. Then a new architecture has been proposed by replacing multiplexer using transmission gate. This approach would provide a solution to reduce the power consumption of carry select adder. In this project, an effective modified area-efficient carry select adder is designed by using transmission gate and finally found out that the modified carry select adder has reduced power consumption and area when compared to basic CSLA .This system is simulated by using MICROWIND tool and the output simulated waveform is analysed..

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