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VLSI MODELING OF SENSITIZATION INPUT VECTOR EFFECT ON PROPAGATION DELAY FOR 32 NM CMOS DESIGNS

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ABSTRACT

As the technology trends keeps on moving with drastic exponential growth the relevant chip level designs are more crucial to support the tendency and the target parameters like area, power and speed are on demand for performance of the chip. As the technology keeps on shrinking beyond deep sub micron levels to reach the target parameters link and power budget is also critical to the designer. On song delay is vital parameter to analyze before the chip went to the application, which cause due to lot of parameters in the chip design cycle. This paper present the effect of input vector sensitization of propagation delay of CMOS circuits at 32 nm technology. The layouts of various test circuits are drawn and modelled using Micro wind 3.1 Simulator.

Index Terms — Link Power Budget, Propagation Delay, Input Vector Sensitization, 32 nm Technology.

I. INTRODUCTION

Design For Testability (DFT), an artistic division of chip level design and development cycle. The DFT deals with estimation and analysis of various test parameters to promote the chip level designs in to the application level. Meanwhile the Timing analysis is the crucial stage of DFT wing of VLSI testing which is used to analyse various Delay models of Chip level circuits which includes both static and dynamic delays for instance rise delay, fall delay, settling delay, switching delay and propagation delay are some of the major issues to be noticed which greatly effects the power consumption of total chip area. Therefore there is a strong desire for every chip level manufacturer to apply chip level Timing Analysis before going to the next stage of testing process.

Timing analysis is a crucial stage in the VLSI design flow whose consequence and difficulty increases with technology scaling because of new physical phenomena appearing in nanometer technologies. The output quantity of the manufacturing process can enlarge considerably using a extremely precise and exact timing analysis tool capable of correctly finding true critical paths, and notice those gates having superior susceptibility to process variations and ecological conditions. As it is familiar that every designer's primitive goal is to achieve as much as possible extent tradeoff between area, power and speed (delay) as a consequence at initial stage a circuit design is synthesized using standard cells, computer-aided design (CAD) algorithms are deliberated to reduce circuit area, power consumption, and propagation delays in adding together with optimization of other parameters. To attain this objective, synthesis tools use library complex gates, i.e., circuit models that come together with primitive logic functions, such as NOT, AND, OR, NAND, NOR, in a single CMOS construction which reduces the number of transistors required to execute a given logic function.

Practically a complex design may be a combination of few primitive functions and extremely large complex functions like high-speed arithmetic units, Multiplexers are also widespread these days CMOS structures. In the perspective of timing analysis, a distinctive nature of complex gates versus basic gates is observed that it is probable to find more than one vector that sensitizes each gate input, while single gates have typically only one sensitization vector. With this document we want to present the gate delay when propagating a transition through a given input of a complex gate may vary considerably depending on the input vector used to sensitize and such

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an input with the subsequent impact on the circuit-level timing computation. This delay variation should not be negligible, being similar to the delay variation caused by process parameter fluctuations.
Generally it is a common practice to the beginner level designers that in the target design if complex gates are existed they are converted to primitive gates prior to timing analysis and then applying the delay model to basic gates and practical designs are suggesting that this kind of approach misleads the design goals as both steps are topologically incorrect and also they performance is also differs with respect to various process considerations. Generally critical path finding algorithms operate in a two stage process which includes essential structural paths and computing their delay later then trying to sensitize repeatedly the highest paths until the critical path is found. Thereby estimating the independent delay for a specific input vector applied to sensitize each complex gate, which may initiate a quite large ambiguity in on the whole delay estimations.

DESIGN DEVELOPMENT

To promote low power high performance applications of CMOS designs chip level delay modeling is essential, various dynamic and static delay modeling Techniques are proposed for timing analysis. The CMOS architectures developed at deep submicron technologies must be analyzed for complete account of propagation delay known as input sensitization vector effect. The proposed article for use of studying the sensitization effect on propagation delay on CMOS designs at 32 nm technology which greatly used to estimate and reduce on chip power consumption adopts the input vector selection condition which results in to dynamic implementation of major techniques.

II. MODELING OF PROPOSED METHOD

In this proposed work, we identified and summarize the effect of the sensitization input vector on the propagation delay for complex gates viewing that delay variations may get up to more than 50% depending on the technology used. Circuit-level analysis predicts that this method has a non negligible effect at the circuit level, being analogous to other effects like parameter variations or wiring load, and summarizes that the dependence of the delay variation with the sensitization vector must be taken into account when performing circuit timing analysis to avoid large ambiguity.
Various test circuits and their layouts are taken into consideration and various input vectors are applied and accordingly the propagation delay has been observed with possible nano meter technologies.

Test Circuit1: four-input ANDOR Gate

Initially a four input ANDOR gate is considered as shown in the figure1 and the corresponding layout is shown in figure2.

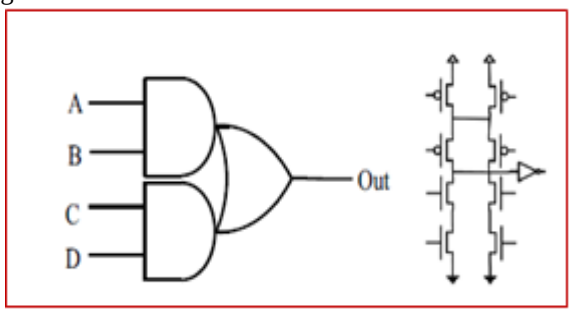

Figure1: Test Circuit1: ANDOR gate

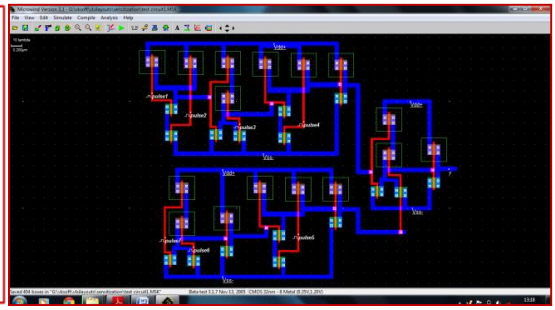

Figure2: Test Circuit1- layout design

Test Circuit2: Three input ORAND Gate

A three input ORAND gate is considered as shown in the figure3 and the corresponding layout is shown in figure4.

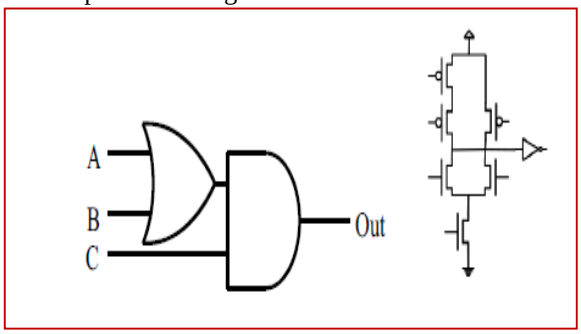

Figure3: Test Circuit2: ORAND gate

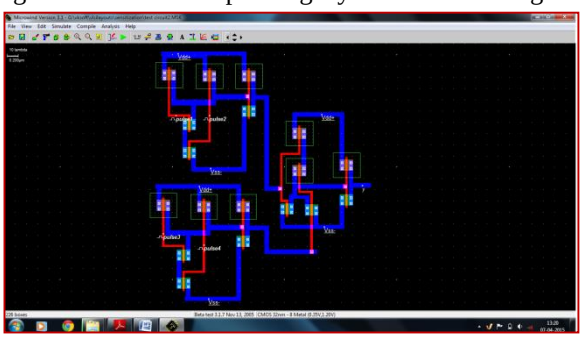

Figure4: Test Circuit2- layout design

Test Circuit3: four input complex Gate

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A four input complex gate model is considered as shown in the figure5 and the corresponding layout is shown in figure6.

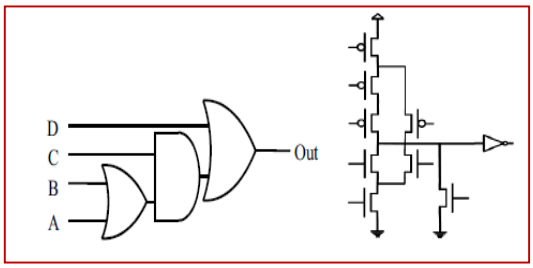

Figure5: Test Circuit3: complex gate

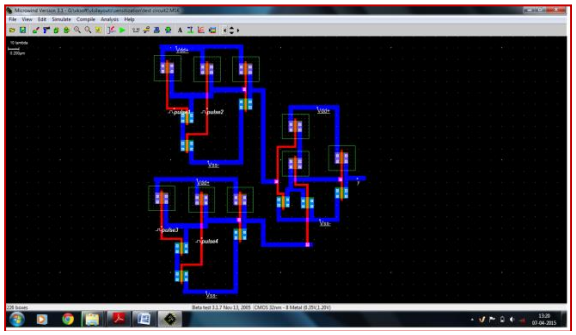

Figure6: Test Circuit3- layout design

Test Circuit4: five input AOI Gate

A five input AOI gate model is considered as shown in the figure7 and the corresponding layout is shown in figure8

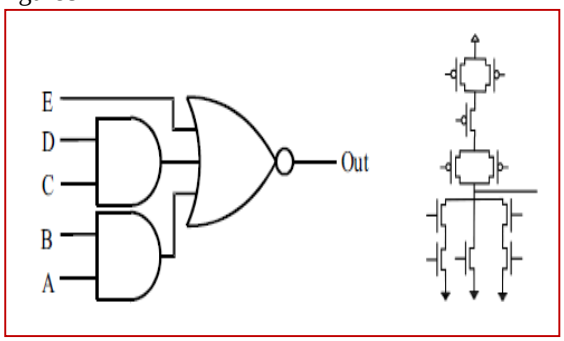

Figure7: Test Circuit4: AOI gate

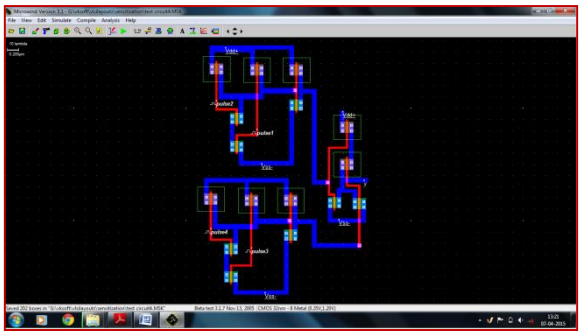

Figure8: Test Circuit4- layout design

Test Circuit5: Seven input complex Gate

A seven input complex gate model is considered as shown in the figure9 and the corresponding layout is shown in figure10

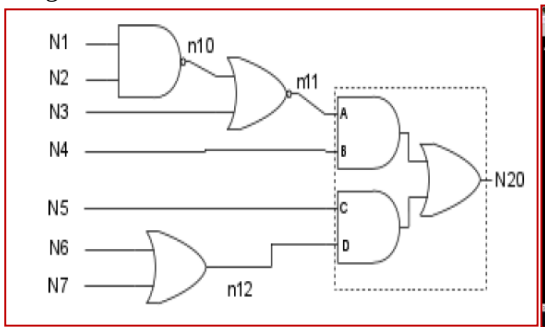

Figure9: Test Circuit5

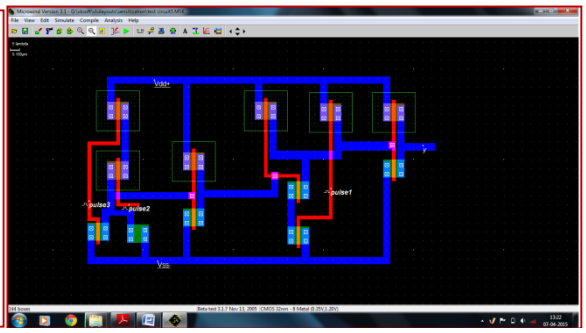

Figure10: Test Circuit10-layout design

III. SIMULATION RESULTS

All the above mentioned test circuits are designed with Micro wind 3.1 simulator with 32 nm technology and the effect of the sensitization vector on the path delay estimation and the simulation results for various circuits and technologies are shown in following figures. It is to be considered that the design supply voltage is constant and is operated at standard room temperature but that parameter of designer's choice can alter as per one's interest.

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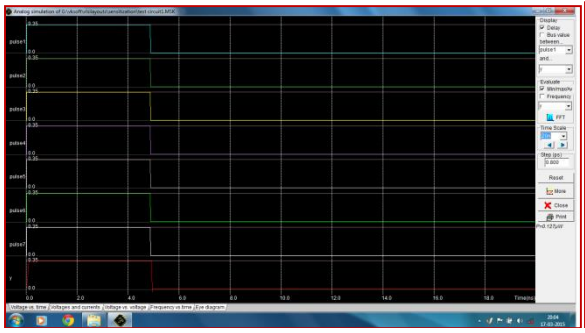

Figure 11: simulation output of test circuit1

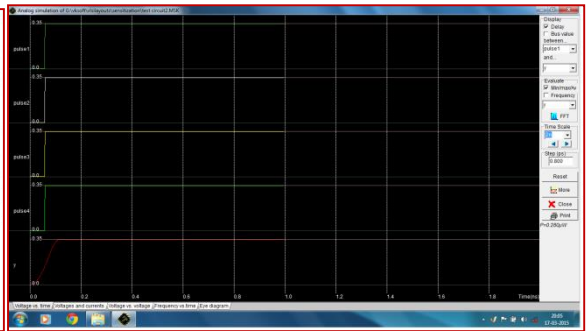

Figure 11: simulation output of test circuit2

Figure 12: simulation output of test circuit3

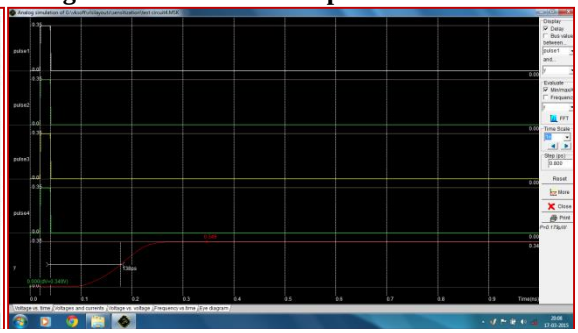

Figure 13: simulation output of test circuit4

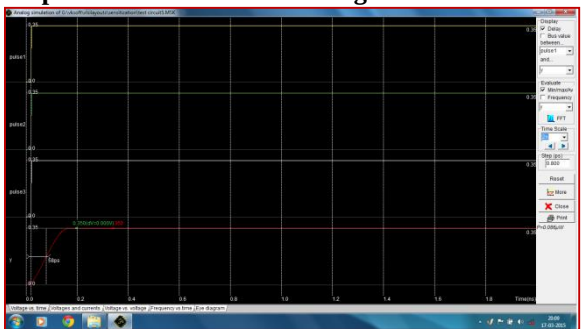

Figure 14: simulation output of test circuit5

The amount of sensitization of input vector on propagation delay (**PD**) for different test circuits are summarized in the following tables

Table1 Characterization of PD-Test circuit4

Input vector	65 nm	45 nm	32 nm
0000	0.080ns	275ps	0.167ns
0001	0.073ns	275ps	0.167ns
0010	0.086ns	275ps	0.123ns
0011	0.089ns	275ps	0.147ns
0100	108ps	275ps	153ps
0101	108ps	275ps	153ps
0110	108ps	275ps	153ps
0111	108ps	275ps	153ps
1000	113ps	286ps	159ps
1001	113ps	286ps	159ps
1010	113ps	286ps	159ps
1011	113ps	286ps	159ps
1100	99ps	245ps	134ps
1101	99ps	245ps	134ps
1110	99ps	245ps	134ps

Table2 Characterization of PD-Test circuit5

Input vector	65 nm	45 nm	32 nm
000	26ps	99ps	43ps
001	26ps	99ps	43ps
010	26ps	99ps	43ps
011	26ps	99ps	43ps
100	27ps	0.059ns	43ps
101	27ps	0.080ns	43ps
110	27ps	0.055ns	43ps
111	27ps	0.057ns	43ps

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1111	99ps	245ps	134ps

Table3 Characterization of PD-Test circuit3

Input vector	65 nm	45 nm	32 nm
0000	18ps	61ps	24ps
0001	18ps	61ps	24ps
0010	18ps	61ps	24ps
0011	18ps	61ps	24ps
0100	18ps	61ps	24ps
0101	18ps	61ps	24ps
0110	18ps	61ps	24ps
0111	18ps	61ps	24ps
1000	18ps	61ps	24ps
1001	18ps	61ps	24ps
1010	18ps	61ps	24ps
1011	18ps	61ps	24ps
1100	18ps	61ps	24ps
1101	18ps	61ps	24ps
1110	18ps	61ps	24ps
1111	18ps	61ps	24ps

Table4 Characterization of PD-Test circuit2

Input vector	65 nm	45 nm	32 nm
0000	0.077ns	3ps	5ps
0001	0.091ns	3ps	5ps
0010	0.056ns	3ps	5ps
0011	0.100ns	3ps	5ps
0100	0.100ns	3ps	5ps
0101	125ps	3ps	5ps
0110	124ps	3ps	5ps
0111	123ps	3ps	5ps
1000	0.064ns	3ps	5ps
1001	124ps	3ps	5ps
1010	123ps	3ps	5ps
1011	122ps	3ps	5ps
1100	0.095ns	3ps	5ps
1101	124ps	3ps	5ps
1110	122ps	3ps	5ps
1111	122ps	3ps	5ps

Table5 Characterization of PD-Test circuit1

Input vector	65 nm	45 nm	32 nm
0000000	18ps	61ps	24ps
0000001	18ps	61ps	24ps
0000010	18ps	61ps	24ps
0000011	18ps	61ps	24ps
0000100	18ps	61ps	24ps
0000101	18ps	61ps	24ps
0000110	18ps	61ps	24ps
0000111	18ps	61ps	24ps
0001000	18ps	61ps	24ps
0001001	18ps	61ps	24ps
0001010	18ps	61ps	24ps
0001011	18ps	61ps	24ps
0001100	18ps	61ps	24ps
0001101	18ps	61ps	24ps
0001110	18ps	61ps	24ps
0001111	18ps	61ps	24ps
0010001	18ps	61ps	24ps
0010010	18ps	61ps	24ps
0010011	18ps	61ps	24ps
0010100	18ps	61ps	24ps
0010101	18ps	61ps	24ps
0010110	18ps	61ps	24ps
0010111	18ps	61ps	24ps
0011000	18ps	61ps	24ps
0011001	18ps	61ps	24ps
0011010	18ps	61ps	24ps
0011011	18ps	61ps	24ps
0011100	18ps	61ps	24ps
0011101	18ps	61ps	24ps
0011110	18ps	61ps	24ps
0011111	18ps	61ps	24ps
0100000	18ps	61ps	24ps

IV. CONCLUSION

In this paper, we have presented a physical modelling of the effect of input vector sensitization of propagation delay of CMOS circuits at 32 nm technology. The layouts of various test circuits are drawn and modelled using

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Micro wind 3.1 Simulator. Such implementations and analysis suggested to exhibits a competitive performance with current work.

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