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VLSI DESIGN OF LOW ENERGY MODELING FOR NETWORK ON CHIP (NoC) APPLICATIONS

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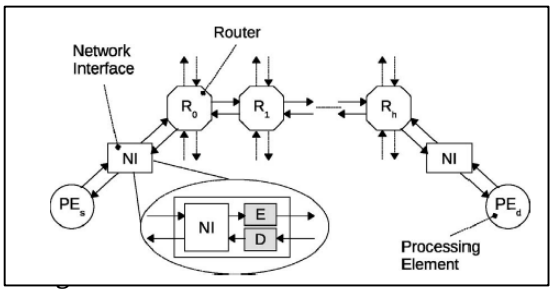
ABSTRACT
As technology trends advances workstation chips become increasingly parallel, an efficient communication substrate is decisive for meeting performance and energy targets, also as nanometre technology shrinks day by day work station chips migrated to SOIC – System On Integrated Chip which leads to too many challenges in the design era, and is more critical for communication applications such as Network On Chip (NoC) and also as technology shrinks, the power supply of NoC links starts to struggle with that of NoC routers. In this paper, we propose the use of efficient data encoding techniques as a practical way to reduce both power dissipation and energy consumption of NoC links. In this work, we target the core cause of network energy consumption through techniques that reduce link and router-level switching commotion. The proposed encoding techniques are simulated and verified by Xilinx tools along with Virtex – 5 FPGA board.

Keywords- SOIC, NOC, Encoding Techniques, energy consumption, Xilinx tools and Virtex -5 FPGA.

I. INTRODUCTION
Despite the fact that process technology scaling continues on condition that more transistors, the transistor performance and power gains that go along with process scaling have largely ceased. Chip multiprocessor (CMP) designs reach greater efficiency than conventional monolithic processors through synchronized parallel execution of multiple programs or threads. As the core count in chip-multiprocessor (CMP) systems increases, networks-on-chip (NoC) present a scalable alternative to conventional, bus-based designs for interconnection between processor cores. As in mainly current VLSI designs, power efficiency has in addition become top-order constraint in NoC design. The energy frenzied by the NoC itself is almost greater than or equal to 28% of the percentile power in the globally referenced standard chip and varies drastically as per the design methodology. As the number of process units of cores integrated into a system on-chip (SoC) increases, the responsibility played by the interconnection unit is also becomes more and more crucial. The International Technology Roadmap for Semiconductors predicts the on-chip communication flaws as the restraining factors for performance and power consumption in current and next generation SoCs. Design in the era of ultra deep submicron technology is mostly conquered by issues concerning the communication architectures. As the design density increases, the total length of the interconnection wires also increases, consequential in long transmission delay and higher power consumption. In accumulation, the space between wires shrinks with technology, increasing coupling capacitance, and the height of the wire material increases ensuing in greater tassel capacitance.
The significant interconnects in complex multi-core chips have escaped from the substance of transistors as a principal factor of performance, power, cost, and reliability. Difficult on-chip communication protocols, involving advanced adaptive routing algorithms, selection policies, data protection schemes, and mechanisms intended at guarantee the quality-of-service are approaching the interconnect system to become one of the main elements which characterizes the system in terms of both power dissipation and energy consumption.



In fact, the recompense over bus-based designs come at the price tag of increase in complexity which pushes the communication system to become one of the main elements of a SoC which strongly impact the cost, power, and performance statistics of the overall system. In general the Network On Chip whose communication links are illuminated as shown in figure1.

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To encounter afore mentioned difficulties instead of physical design variations various data encoding schemes had been proposed and literatures are suggested that these encoding techniques are results with hardware overhead which interns creates disturbances in the system performance because of switching activity which is the root cause in the network links the proposed data encoding technique for NoC can be a counter measure to above problem and suggested to be a good approximation to current trends of NoC technology.

DESIGN DEVELOPMENT

To promote low power high performance applications of NoC, Various Data encoding Techniques are modeled on VLSI. The VLSI architectures developed as follows

The VLSI architecture of data encoder for NoC to reduce on chip energy consumption adopts the bit inversion condition which results in to three major techniques as the inversion is evenly based, oddly based or fully inverted condition of the data being encoded for target NoC. All these techniques are modeled and implemented by targeting flit occurrence probabilities of the transistor devices. The next proceeding section will conclude all the proposed schemes. This proposal is also realized into field programmable gate array (FPGA) prototyping system using Xilinx Viitex-5 unit. The maximum operating frequency of this design is more than 500 MHz.

TABLE 1
SUMMARY OF DESIGN CONSIDERATIONS

S.no	Design consideration	Selection
1	Compiler	Xilinix14.4Vivado
2	Programming Language	Verilog
3	FPGA	Virtex -5
4	Interface	USB

II. MODELING OF DATA ENCODING TECHNIQUES

The fundamental approach of this idea is to encode the flits before they are involved into the network with the objective of reducing the self-switching action and the coupling switching activity in the links traversed which is identified as a root cause of link power dissipation throughout the Chip area. The data encoding techniques can be divided into two types. In the first type, encoding procedure focus on diminishing the power due to self-switching activity of individual bus lines while ignoring the power dissipation due to their coupling switching activity. In the second type Gray code encoding was suggested for the case of concurrent data patterns. Yet this type of encoding mechanisms are not sustainable to deep sub micron process where the switching capacitance may leads to un necessary and un avoidable energy dissipation and some time introduces as an error whenever there is a transition between data values with either 1 →0 or o →1 known as flit and is dominant and becomes more critical if the data size increases.

Flit model across transistor:

The number of transitions from 0 to 1 for two successive flits (the flit that immediately traversed and the one which is concerning to traverse the link) is counted. If the number is greater than half of the link width, the inversion will be performed to reduce the number of 0 to 1 transitions when the flit is transferred via the link. This technique is only concerned about the self-switching without disquieting the coupling switching. Note that the coupling capacitance in the state-of–the-art silicon technology is significantly more when compared with the self-capacitance and therefore the data encoding technique must be centralized with link power reduction for NoC. Hence recall that the observation that the entire encoding scheme will be dependent on count of flit inversions which may be an even or odd and whose effects are shown in the following tables.

TABLE2 EFFECT OF ODD INVERTED FLIT MODELS

Time	Normal			Odd inverted		
	Type I			Types II,III,and IV		
t-1 t	00,11 10,01	00,11,01,10 01,10,00,11	01,10 11,00	00,11 11,00	00,11,01,10 00,11,01,10	01,10 10,01
	T1*	T1**	T1***	Type III	Type IV	Type V
t-1 t	Type II 01, 10 10, 01			Type I 01, 10 11, 00		
t-1 t	Type III 00, 11 11, 00			Type I 00, 11 10, 01		
t-1 t	Type IV 00,11,01,10 0011,01,10			Type I 00,11,01,10 01,10,00,11		

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TABLE3 EFFECT OF EVEN INVERTED FLIT MODELS

Time	Normal			Even inverted		
	Type I			Types II,III,and IV		
t-1 t	01,10 00,11	00,11,01,10 10,01,11,00	00,10 01,10	01,10 10,01	00,11,01,10 00,11,01,10	00,11 11,00
	$T1^{*}$	$T1^{**}$	$T1^{***}$	Type II	Type IV	Type III
t-1 t	Type II 01, 10 10, 01			Type I 01, 10 11, 00		
t-1 t	Type III 00, 11 11, 00			Type I 00, 11 01, 01		
t-1 t	Type IV 00,11,01,10 0011,01,10			Type I 00,11,01,10 10,01,11,00		

Reference power model:

The dynamic power degenerated by the interconnects and drivers is

$$P_D = [T_0 \rightarrow 1\ (C_s + C_l) + (Tc)\ (Cc)]\ V^2_{dd} F.$$

Where $T_0 \rightarrow 1$ is the number of $0 \rightarrow 1$ transitions in the bus in two consecutive transmissions, *Tc* is the number of correlated switching between physically adjacent lines, *Cs* is The line to substrate capacitance, *Cl* is the load capacitance, *Cc* is the coupling capacitance, V_{dd} is the supply voltage, and *F* is the clock frequency. Depends on this power model three types of data encoding techniques are proposed as discussed here after

Encoding Technique1:

This encoding technique uses the principle of reducing the Type I flits in to Type III or type IV and Type II flits converts into Type I the proposed architecture for this technique is shown in figure2.

Encoding Technique2:

In this technique the data encoding mechanism includes both odd and full inversion. The full inversion operation converts Type II transitions to Type IV transitions; the relevant architecture is shown in the figure3.

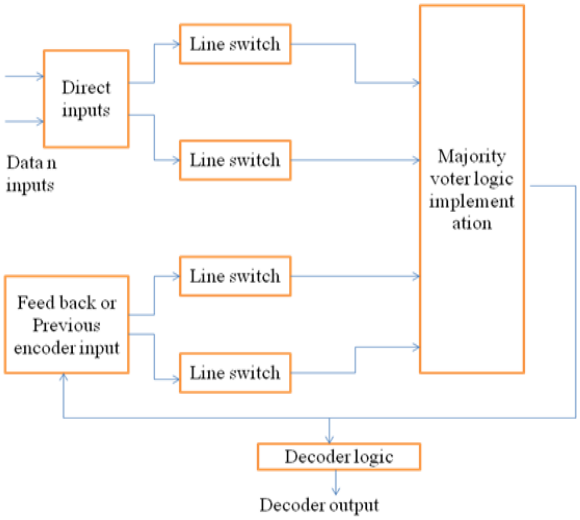

Figure2: Block Diagram of Encoding Technique 1

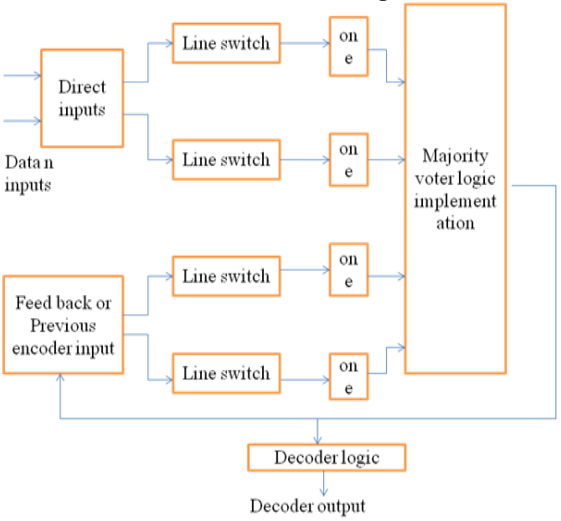

Figure3: Block Diagram of Encoding Technique 2

Encoding Technique3:

It is assumed that the even inversion may diminish the link power dissipation , and hence in this technique we include even inversion to encoding technique2 since the odd inversion converts some of Type I transitions to Type II transitions. And the proposed block diagram is shown in figure4.

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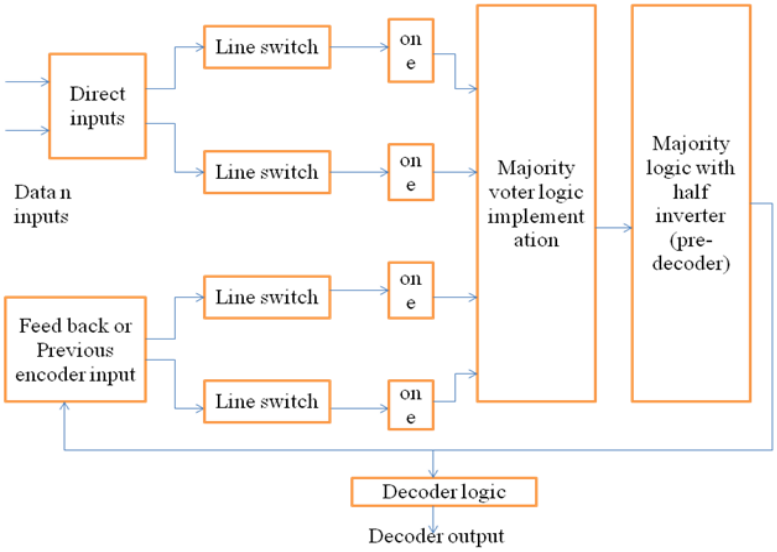

Figure4: Block Diagram of Encoding Technique 3

Front-End Modeling:

This phase of implementation contains the following stages simulation using Xilinx 14.4 Vivado suite, synthesis using Xilinx 14.4 XST and verifying on Virtex – 5 FPGA board.

III.SIMULATION AND SYNTHESIS RESULTS

The Verilog RTL Description of the above article is simulated and synthesized using Xilinx14.4 (ISE-Simulator), implementation of all the above encoding techniques are successfully synthesized and verified on Virtex -5 FPGA board and the results are shown below.

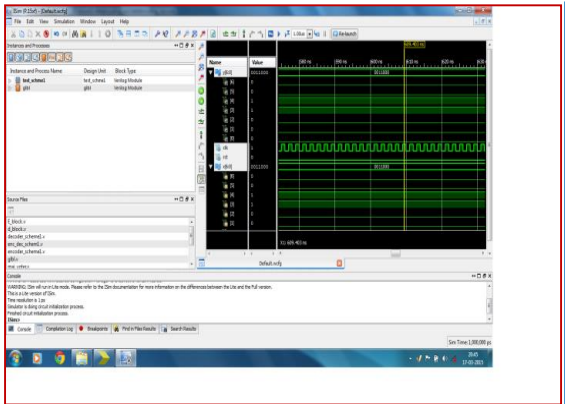

Figure5: Simulation output of Technique1

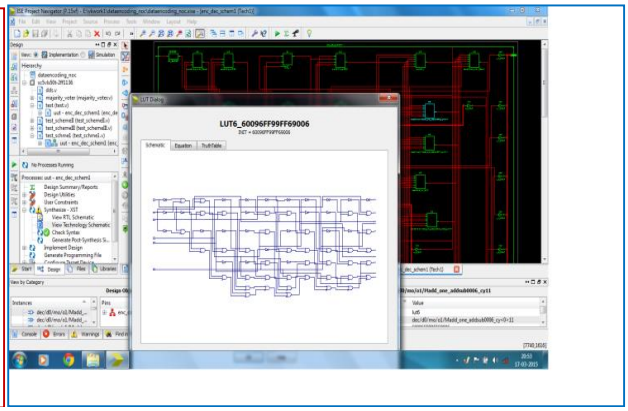

Figure6: Synthesis output of Technique1

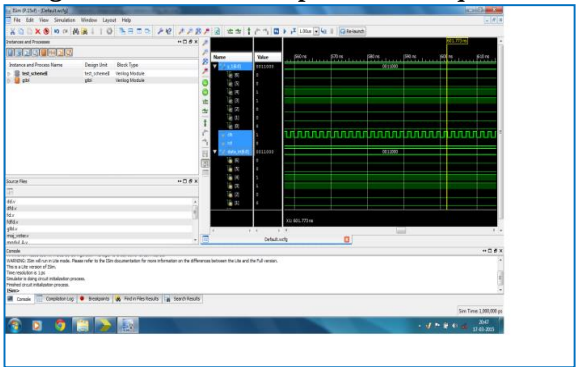

Figure7: Simulation output of Technique2

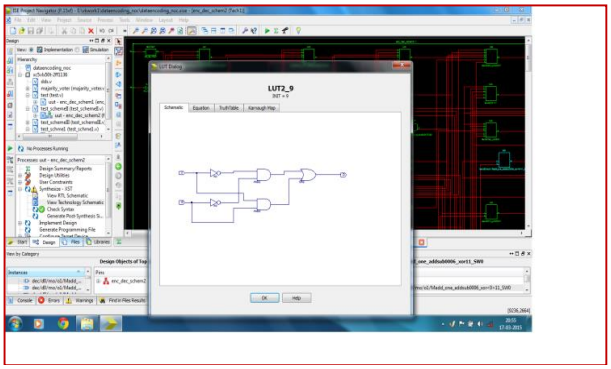

Figure8: Synthesis output of Technique2

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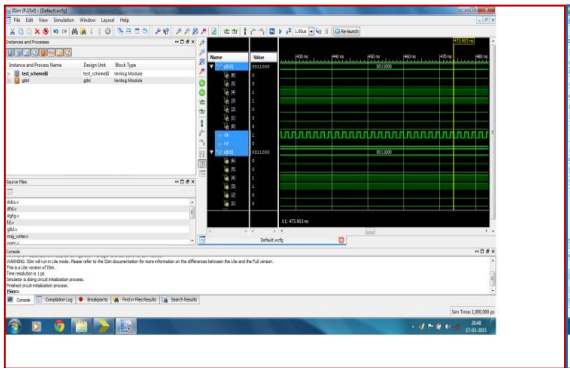

Figure9: Simulation output of Technique3

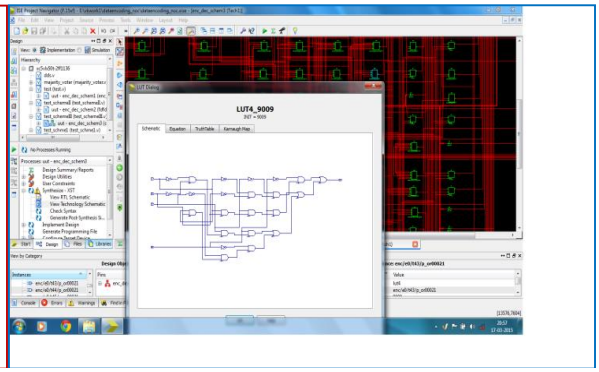

Figure10: Synthesized output of Technique3

The Synthesized report is summarized in the following Table.

TABLE 2 SUMMARY OF SYNTHESIS REPORT

S.no	Parameter	Technique1	Technique2	Technique3
1	Target Device	xc5vlx50t-2-ff1136	xc5vlx50t-2-ff1136	xc5vlx50t-2-ff1136
2	Slice Logic utilization	Less than 5%	Less than 5%	Less than 5%
3	Slice logic distribution	87%	81%	87
4	IO utilization	3%	3%	3%
5	Specific feature factor	3%	3%	3%
6	Total logic delay	9.093 nS	8.097 nS	9.093 nS
7	Total offset delay	9.592 nS	7.200 nS	11.527 nS
8	Total path delay	9.592 nS	7.200 nS	12.026 nS
9	Real time compilation	14 S	12 S	16 S
10	Total memory usage	287724 Kb	285032	287728

CONCLUSION

In this paper, we have presented VLSI modelling of set of novel data encoding techniques designed at reducing the power dissipated by the links of a NoC. In actuality links are responsible for a significant portion of the overall power dissipated by the communication system. In addition, their part is usual to increase in potential technology nodes. this paper has realized with Xilinx tools along with Virtex -5 FPGA. Such designs are suggested to exhibits a competitive performance with current work.

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