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PERFORMANCE OPTIMIZATION APPROACH FOR ADDER IN FOLDING TREE ARCHITECTURE

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ABSTRACT

Performance optimization design requires recurrence technique, effective algorithm, less power dissipation with delay trade-off and minimum area with fewer congested wires. In this paper, the new architecture is proposed for parallel adder and the performance of the parallel adder is analysed and compared with the various parallel adder. Architecture logical elements is reduced by avoiding the input carry to propagate in the architecture. Folding technique increases the probability of designing complex architecture with less logic elements. Various adders and proposed work are also examined in 8, 16 and 32 bits to obtain the performance of an adder in minimum and maximum complexity in the region. By analysing adders in various bits, the performance of the proposed work is better compared with various parallel adders. Power consumption is reduced by 12-15% as compared with the existing algorithms using Cyclone III (EP3C16F484C6) and SYNPLIFY 9.6.1.

Keywords: *Folded Tree Architecture (FTA), Parallel Prefix Operation (PPO), Processing Element (PE), Ladner-Fischer Adder (LFA).*

1. INTRODUCTION

Digital devices have become part of our everyday life. Though most of the physical quantities are analog in nature like temperature, force, position and pressure, we process that quantity in digital only because digital technology has numerous advantages than analog technology [4]. Some of the advantages of digital over analog are noise immunity, higher accuracy, storage of data is easier and simpler to design. This makes digital signal processor popular in today's environment. The analog quantities can process in the digital system with the help of converters. Analog-to-digital converter is used at both input and output. The intermediate process is carried out by the digital quantities and devices. [10]

There are several ways to reduce power in the digital system, but the easy way to reduce power in the digital system is to reduce the number of components used to perform the certain operation. This type of reduction not only reduce the power require to process but also reduce the area and heat produced by the processor. All the digital systems can make by combinational and sequential logic circuits. Part of sequential logic circuit can make combinational circuits. The basic element in combinational design is adder. Any type of digital signal processing circuits to perform certain operation like subtraction, division and multiplication can be made with the help of adder. So the performance of the system is relatively dependent on adder performance. If the performance of adder increases, system performance also increases. Basically adder is designed by logic gates. By reducing the number of logic gates needed by the adder to perform an operation then area is reduced which in turn reduces the power used by the adder. The delay used by an adder can also be reduced by reducing the propagation time and waiting time of logic gates for previous result. Mostly parallel adder is used in all applications because it doesn't wait for the previous carry to propagate which reduces the delay in circuit. But it requires large number of logic gate to perform the operation. Some of the existing parallel adders are CLA (Carry Look-ahead Adder), CSA (Carry Save Adder) and Ladner Fischer adder [15].

Operation of CLA leads to increase of area which leads to reduced delay when compared to CSA. The disadvantage of CSA is decrease in area with help of increased delay. Compared to other adders Ladner Fischer adder perform effectively. Proposed adder is introduced to reduce delay, area and power compared to all other existing adder used. Proposed adder is designed by changing the logical element in Carry Look-ahead Adder. The area of adder can reduce even more by introducing folded tree architecture in the adder block. This reduction in area, power and delay optimize the performance of adder.

This proposed architecture can widely be used in all types of application which performs an operation related to addition, subtraction multiplication and division. Some of the applications are wireless sensor nodes, data-acquisition system [1], FFT and other application, which use Digital Signal Processor. In FFT, it is used to perform the complex addition and multiplication operation [2]. The important advantage of proposed system is that it has reduced power consumption in power constraint devices. The outline and subsequent sections have been discussed below.

Section II describes about the analysis of various literature survey used to implement the proposed system, and Section III presents parallel adders used in contemporary digital environment. Work which is proposed in DSP architecture is described in Section IV. Section V describes the performance parameters of the adder. In Section

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VI, adder's simulation results with its performance analyze is carried out. In Section VII, clarifies about the conclusion and future work of paper.

2. RELATED WORK

Roy *et al*. [7] provides performance area trade-off by introducing an efficient algorithm. The main objective is to reduce the size of the prefix graph. There are two designs in selecting the parallel prefix structure; they are custom and automatic synthesis. The performance of automatic synthesis is less compared to custom synthesis. In the parallel prefix structure, complexity increases exponentially based on the number of bits. By reducing the size the proposed system can process more complex situation compared to the existing system. Designing more size-optimal solution makes each to choose the size depend on power consumption and wire congestion. The performance of the prefix structure is increased by 3%, and the area is reduced by 9%. *Vikramkumar Pudi and K. Sridharan* [16] presents proficient QCA schemes for various adders. The parallel adder used in this design are ripple carry adder, Ladner-Fischer adder, Brent-Kung adder and so on. *Vikramkumar Pudi and K. Sridharan* also proposes new architecture for Brent-Kung adder which provides low complexity on QCA design. A three operant binary addition process is introduced by *Sabyasachi Das and Sunil P. Khatri* to reduce the performance and area trade-off and reduce the depth of the adder [3]. This operator will merges the three adjacent blocks to calculate propagate and generate signals of the blocks. To perform this process classical two operator adder and ripple carry adder is used. This system is faster than other parallel adder but this consumes large amount of area. In theoretically folding network is works well with the tree like structured networks. But though this works well with this network there are many limitations in the folding network which are analyzed by *Barbara Hammer* [9]. To analyze the folding network two separate approach s taken. One is the size of the tree is limited before starting the process and other one is limiting the input height of the tree. This paper [11] introduces an adder which is designed using two adders to provide better performance in power. Though this adder provide solution to the power problem, it has major disadvantage. The adder can use only even number of CMOS stages which leads to area problem. In Paul et al. [12] paper single transistor cell is used to design a ROM with less number of logical elements by reducing the identical columns and rows. Though area is reduced the power utilized by the device is increased.

3. STUDY OF ADDER DESIGNS

3.1 Carry Select Adder

Carry select adder uses ripple carry adder with multiplexer to reduce the area require to perform the parallel addition operation. Mainly, this is introduced to overcome disadvantage of carry look-ahead adder which is area. To perform n-bit arithmetic operation two n-bit ripple carry adder is multiplexed. Former is used for carry-in to zero while later is computed with carry-in to one. Once exact carry is known one of the product is selected from two product [7]. Due the waiting for a carry in there exists an area-delay trade-off. When delay increases, area reduces and vice versa. It provides better performance compared with CLA. It is used in many data processing processors. Fig. 1. Shows the architecture of carry select adder. Time delay is equals to addition of computational time taken for first section and selection of sum depend upon the carry from subsequent section.

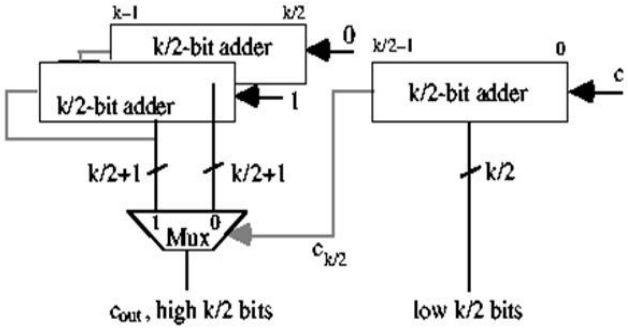

Fig.1. Carry select adder

Equations,

Addition is carried out by ripple carry adder,

$$sum = A \oplus B \oplus C_{in} \quad (1)$$

Two operations carried by considering,

C_{in}= 0,

$$sum_0 = A \oplus B \oplus 0 \quad (2)$$

C_{in}= 1

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$$sum_1 = A \oplus B \oplus 1 \quad (3)$$

Multiplexer is used to select the product based upon previous carry,

$if\ C_{in} = 0$

$select\ sum_0$

$else$

$select\ sum_1$

3.2 Carry Look-ahead Adder

Carry look ahead adder is introduced to perform addition operation simultaneously without waiting for previous carry (to determine carry signal in advance depending on input signal). There by, it execute fast compared with other adder. It can split into two blocks, one is used to generate carry generation and propagation terms, and other is used to produce the carry out without waiting for previous carry [6]. Sum bit is readily available after single gate delay. The delay is same for any number of bits to be added. So, this adder is useful when number of bits to be added is higher. Fig. 2. Shows the single bit operation of carry look-ahead adder. It cannot be used for larger bits due to limitation of area. It requires large area for addition compared with other adders.

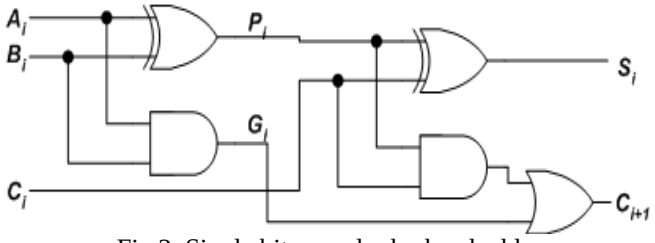

Fig.2. Single bit carry look-ahead adder

Boolean equations,

$$P_i = A_i \oplus B_i \quad (4)$$

$$G_i = A_i * B_i \quad (5)$$

$$S_i = P_i \oplus C_i \quad (6)$$

$$C_{i+1} = G_i + P_i C \quad (7)$$

Propagate and generate term will depend on input bits.

3.3 Other Adder

To improve the performance of adder, a triple carry operator is introduced which is combination of carry look-ahead adder and parallel prefix adder [13]. This triple carry operator performs propagate and generate operation for three adjacent blocks simultaneously. By doing this operation the performance of the adder is increased. Fig. 3. shows the triple carry operator.

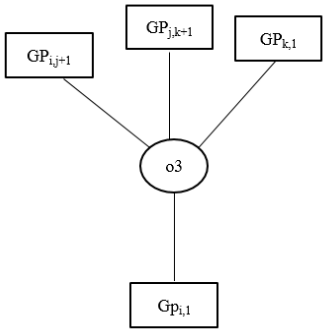

Fig.3. Triple carry operator

In the following section the folding tree architecture and the structure of proposed adder with parallel prefix structure is explained.

4. FOLDING TREE ARCHITECTURE AND MODIFIED PARALLEL ADDER

Folded tree architecture is used to reduce the area needed by the processor to process the operation. This will reduce the power needed by the system because the area is proportional to power.

4.1 Folded Tree Architecture

Blelloch's approach of binary tree implementation requires p=n-1 processing elements to process n inputs. The

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number of inputs used by a binary tree implementation can be brought down by introducing the pipeline process in it [14]. However, when the pipeline process is introduced, it will degrade the output to some extent. A binary tree will divide the process into several layers depend on the number of stages used, and once it completes a layer, it will process the new inputs and produce the new outputs [8]. By using such a way the reusability of processing element increases. The folding tree architecture is similar to binary tree and reduce the number of processing elements in half thereby reduce the area used to process the operation. When area used by the processor is reduced, it reduces both the power and wire length used. Fig. 4. shows the folding architecture [9]. FTA uses combination of control and data flow elements, which improves flexibility by avoiding the bottleneck problem. The main elements which are used to perform folded tree operations are PE array, iteration count, memory, buffer and Finite State Machine. The PE contains the operation of the circuit. Folding of processing element is done with the help of other elements. Counters and FSM are used to reuse PEs.

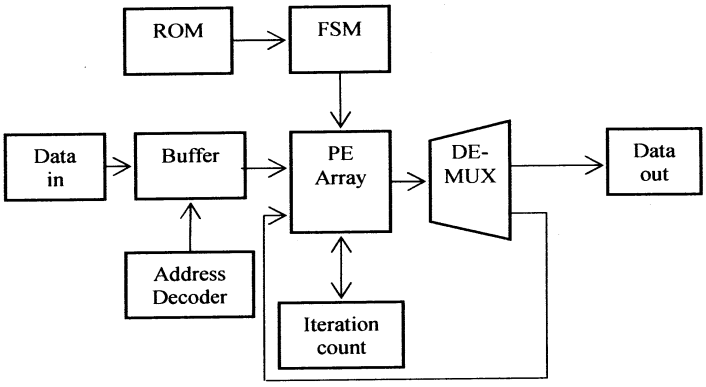

Fig.4. Folding architecture

FSM will provide the iteration count to the PE based upon the instructions given by the programmer. The counter will count the iteration count. Once the final count value is reached, then FSM will stop to provide iteration count value and produce the desired output. Depend on the application, PE will change, which changes the structure.

4.2 Parallel Prefix Structure

An adder is the most basic component in a digital system. All digital system needs adder because we can perform any type of digital operation with the help of an adder like subtraction, multiplication and division [3]. When optimizing the performance of the adder in the digital circuit, we can optimize the performance of the circuit. The main parameters which decide the performance of the digital circuits are area, power and delay [5].

4.3 Modified Parallel Adder

CLA performs addition fastly, but simultaneous propagation of carry bit increases the area used by CLA. Increase in the area leads to increase in power because each gate has its own amount of power dissipation. Each gate will dissipate some amount of power when number of gates used in the circuit increases the power, increases the dissipation [17]. The power utilized by carry look-ahead adder can reduced, by avoiding the input carry which is Modified Parallel Adder and its least two bits operation is shown in Fig. 5.

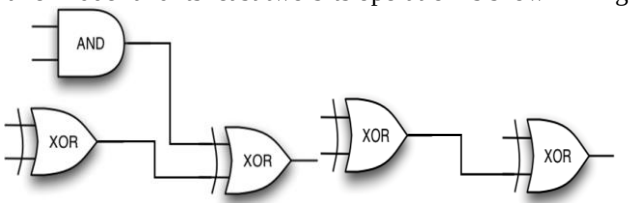

Fig.5. Least two bits addition operation in MPA

5. EXPERIMENTAL VALIDATION

Power is one of the parameters, which is applied to examine the performance of all DSP devices. There are two types of power exist in circuits; they are static and dynamic power.

5.1 Static power

Initially, there is no switching activity takes place in a transistor. Even though there is no switching takes place, a small amount of power is continuously dissipated by the transistor which is said to be static power.

$$P_{stat} = I_{stat} * V_{DD} \quad (8)$$

where, I_{stat} and V_{dd} are static current and supply voltage of the transistor. The supply voltage and ground will decide the ON and OFF of the transistor. That is, when the transistor switch is connected to supply voltage then PMOS transistor turns ON and when it is connected to ground NMOS transistor turns ON.

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5.2 Dynamic power

Dynamic power is produced by transistor when there is a switching in the input occurs.

$$P_{dyn} = C_L V_{DD}^2 P_{0\to1} f \quad (9)$$

Transistor size and wire length will decide the C_L value. By reducing the C_L value, higher performance is archived. The value of supply voltage (V_{dd}) will drop continuously as transistors stage increases. $P_{0\to1}$ tells about switching activity of the transistor which is said as an activity factor. Clock frequency (f) is decided by the processor. So, the processor is also a parameter which changes the dynamic power dissipation of the transistor.

Table 1. contains information about the power dissipation of various adders. Power dissipation in proposed adder is 95.23mW which is comparatively less with other adders. Power dissipation increases when there is an increase in the number of input bits.

Table 1. Power dissipation of various adders

1 processing element	Existing system	Proposed system
Dynamic power dissipation(mW)	8.06	6.31
Static power dissipation(mW)	46.17	46.16
I/O power dissipation(mW)	43.35	42.76
Total power dissipation(mW)	97.58	95.23

5.3 Area and delay

The operating frequency of the device is also an important parameter in a digital environment. The frequency will decide the dynamic power dissipation and delay of the gates. When the operating frequency increases it will increase the power dissipation and reduce the delay. So, optimization is required in frequency to maintain power and delay tradeoff. There are two ways to optimize the performance. One is by selecting the correct device to perform an operation. We can optimize the performance. Another is by reducing the number of logic gates or area of the circuit, we can optimize the performance of the device. The delay of the overall circuit can be reduced by changing the frequency of the device. The frequency is inversely proportional to delay. The following equation shown the relation between the frequency and delay,

$$time = 1/\ frequency \quad (10)$$

6. RESULT AND ANALYSIS

The various existing adders and proposed architecture is designed using Verilog hardware description language (Verilog HDL). Both existing and proposed adder process the same input, which is easy to analyze various parameters, which decide the performance of the adder. Fig. 6. shows the output of an adder which is simulated using MODELSIM and Fig. 7. shows the simulation result of polar encoding and decoding using MODELSIM. The performance of various adders is analyzed, using FPGA family CYCLONE III and device EP3C16F484C6. To get the detail analysis about the area and delay of the adder, SYNPLIFY 9.6.1 is used.

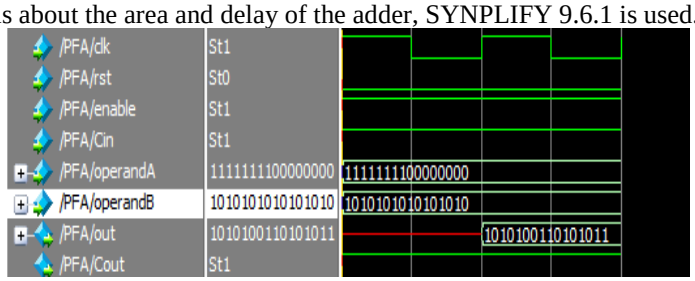

Fig.6. Operation of Modified Parallel adder

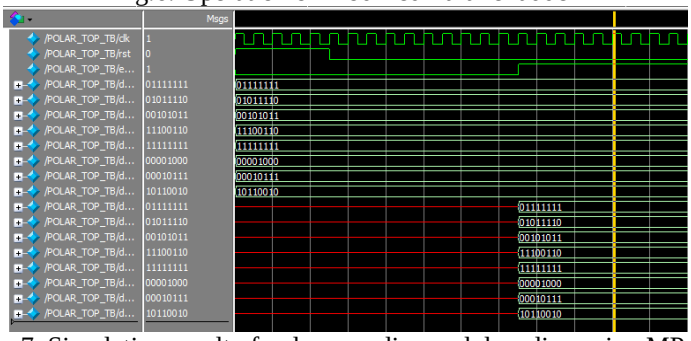

Fig.7. Simulation result of polar encoding and decoding using MPA.

Fig. 8. and Fig. 9. shows the comparison between parameters of various adders which is used to analyze the performance of the adder. Adders used in the comparison chart are Carry Look-ahead Adder, Carry Select Adder, Ladner Fischer Adder and Proposed Adder.

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Table 2. shows the area analysis of various adder with the proposed adder. The proposed adder contain the less number of logic gates compared with the other two adder designs. This reduced number of logic elements will improve the performance compared with other two adders.

Table 2. Area analysis of various adders with proposed adder

	CLA	RCA	MPA(Proposed Adder)
Core cells	302	424	198
IO cells	53	53	52
Total	355	477	250

Table 3. shows the frequency analysis of various adder with the proposed adder. The frequency of adder will determine the speed of the circuit. So, the adder should work on high frequency to optimize the speed of the device. The proposed adder is efficient in performance by working in high frequency and also being faster in execution.

Table 3. Frequency analysis of various adders with proposed adder

	CLA	RCA	MPA(Proposed Adder)
Requested frequency	77.7	99.8	109
Estimated frequency	66	84.9	92.6

Table 4. shows the delay analysis of various adder with the proposed adder. The total path delay of the circuit is calculated using propagation time, setup time, intrinsic clock delay at the starting point and ending point. Once the total path delay is reduced the device performance is optimized. Logic delay is the delay produced due to logic gates in the circuit and route delay is the delay produced by the propagation of the signal from input to output. Proposed system has less logic and route delay compared with the other existing adders and hence being efficient in performance.

Table 4. Delay analysis of various adders with proposed adder

	CLA	RCA	MPA(Proposed Adder)
Logic delay	1.592	1.655	1.504
Route delay	13.550	10.130	9.290
Total path delay	15.142	11.785	10.794

From the above comparison, it is clear that the proposed work is effective compared with other work. Each adder will perform differently based upon number of bits used as input. From the result obtained it is clear that the area and power of proposed system is comparatively less with existing system.

CONCLUSION

This paper presents the architecture which is used for many low power applications. Some of power needed applications are Wireless Sensor Network, Data Acquisition System, Laptop, and Application which are in mobile in nature. The power used in this architecture is reduced by changing the internal architecture of processor. The internal architecture is changed with help of adder. In existing carry look-ahead adder is used. The power utilized by that is large due to large logic gate used. So, by changing that internal block the power used by the system can be reduced. In proposed, carry input given to the CLA is neglected. By neglecting the carry input the logic elements used by the architecture is reduced thereby power is reduced. Proposed system can reduce the power up to 10% compared with existing system. In future, the architecture can be optimized by changing the clock distributed across the whole architecture. By changing the clock distribution network the speed and power used by the architecture can be effectively optimized.

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