Vol 06, Article 06601; June 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

AN EFFICIENT VOLTAGE COMPARATOR USING PREAMPLIFICATION PROCESS

R.PRASHANTH[1], K.GOMATHY[2]
[1,2] Department of Electronics and Communication Engineering, Velammal Institute of technology, Panchetti, Chennai, India.
[1]rprashanth.si12@gmail.com, [2]gomathyvasantha@gmail.com

ABSTRACT

Comparators are the basic building electronic component for designing analog and mixed signal systems. The comparators are used to compare the current or voltage and to produce the outputs indicating which is larger. Power and area are the two most important factors which are required for high speed applications. In this, a comparator is designed as a preamplifier based in which, the total number of transistors is reduced to provide the result more efficient with glitch free By replacing these transistors, the area of the circuit gets reduced and hence the power. Also, the propagation delay gets reduced. The simulation results of the pre-amplifier based clocked comparator shows that it has reduced power dissipation and minimum logic elements. This has an application on PWM and can be used in ADC's for accessing more than 8 bits by implementing in a parallel prefix structure.

Index terms: boost-up transistors, double tail comparator, propagation delay, pre-amplifier based comparator, logic elements, PWM, parallel prefix structure.

1. INTRODUCTION

The comparator is a device which is used to compare two current or voltage and in turn produce the output as a digital signal indicating which is larger with reference to a masterpiece. The comparators are mainly used in ADC's. It can be employed in batch production where a very fast rate of components to be checked and to arrive at the production line move quicker. To inspect recently purchased gauges, it can be applied. Comparators are classified into many types, some of them are mechanical comparator, electrical and electronics comparator, multi check comparators, automatic gauging comparator.

In aeronautics, ultrasonic machining, applications the comparator can be applied where the comparator consumes more power, so the battery will be used more and so there exists replacement of batteries often. The replacement in batteries reduces the life of the component. Therefore a comparator is designed which increases the life of the shelling by consuming less power.

2. RELATED WORKS

For all comparator architectures, the latched comparator virtually forms the basic building block [1] which regenerates the analog input signal into the wide scale level of digital signal. For this it uses the mechanism called positive feedback mechanism. The potential fluctuations are present in the input signal. These fluctuations affect the input voltage producing a noise called kick back noise. This latched comparator is designed primarily to reduce the kickback noise which increases the power dissipation hence this CMOS latched comparator is designed to reduce the kickback noises.

[2] Describes about the low power, low voltage design of SAR ADC. A technique called supply boosting technique (SBT) is used. This sheds light on the importance of SBT and supply boosted circuits (SBC). The SBT is used for designing applications for energy constrained systems. This technique steps out a 147nW consumption of power. The so obtained design of SBC can be used in the shift registers of any type and uses a full scale input range.

Paper [3] describes about the need of A/D converters. For dynamic, regenerative comparators, to maximize the efficiency in both power and speed, this paper is based on. This mainly explains about the analysis of area and power in which the conventional double tail comparator is modified to function in low power applications by introducing a few transistors. A technology of 180nm CMOS is proposed which reduces the power consumption in the order of 10^-6 Watts.

[4] Presents about a modified conventional latch type comparator which operates in small voltage of 0.65V.This has a better output swing, high impedance input and maintaining no static power consumption. This is manufactured in 65nm CMOS technology. Compared to voltage sense amplifier [9], the proposed comparator design shows a good sensitivity, speed and trade away.

[5] Proposes a comparator that requires one phase clock. A low input noise is held about three times more depressed than the conventional comparator. This achieves about 1.69MV offset and has an effective comparison of potential differences. It can compare 1.0mV at frequency range of 1GHz. An efficient self

Vol 06, Article 06601; June 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

calibrating technique is used. This technique is used for acquiring low offset voltage and area. By using sub micron CMOS technology this is achieved.

[6] Describes about a supply boosting technique which is desirable for low power clocked circuits amplifiers and level shifters. A unique clock booster is designed and uses input common mode of supply boosting comparator range. The energy efficiency from the boosted supply is caused due to this common mode use of the inputs.

3. EXISTING SYSTEM

3.1 Double Tail Latch Comparators

The circuit and schematic diagrams of the comparator presented in [3] are shown in Fig. 1. This comparator is compared with dynamic latched comparator design because of its speed and suitability for low supply voltage applications. It operates in 2 phases 1) Reset phase 2) Regeneration phase. While the clock is low(reset phase), M7 and M8 transistors are ON. M9 transistor is off. As M7 and M8 transistors are ON Di+ and DI- nodes are recharged to Vdd. So M10 and M11 become ON and discharge the output nodes OUT+ and OUT- to ground.

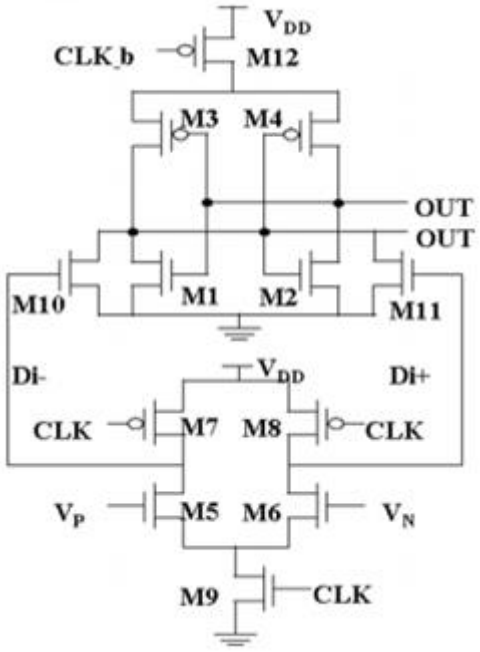

Fig. 1 Double tail comparator

When the clock is high (regeneration phase), M7 and M8 transistors are in OFF state. M9 and M12 transistors are in ON condition. So Di nodes start to discharge as M9 turns ON. As Di nodes start discharging, M10 and M11 are initially in ON condition and gradually M10 and M11 becomes OFF. The difference between voltages of Di+ and Di- (ΔVDi) are given to M10 and M11 transistors. Output nodes OUT+ and OUT- starts regenerating when M10 and M11 are unable to ground the outputs. The intermediate stage formed by M10 and Mll passes ΔVDi to the cross-coupled inverters and also provides additional shielding between the input and output, with less kickback noise as a termination.

3.2 Dynamic Latched Comparator

There are two stages of dynamic latched comparator. Except two cross coupled inverters all the transistors operate in the first stage called as interface stage. The two crosses coupled inverters are operated in the second phase, which is called as regenerative stage, at this stage each input is related to the production of some other. Clock can be low or high. When it is low, tail transistor is off and VDD or ground is given to output based upon the closed connection of Vp and Vn. In another clock value the output discharge to ground. Time lag and power can be thinned out using dynamic latched comparator circuit compared with other comparator. Power use is cut back in double tail latched comparator, but the velocity of the comparator is low due to more transistor count. High speed is archived in pre amplifier based clocked comparator, but the power consumption of the comparator is high because it uses an amplification stage. Use of static power in comparator is high during amplification period. Nevertheless, since the pre-amplifier based clocking comparator is to exercise at high frequency, the energy use of the pre-amplifier based clocking comparator becomes comparable to the double tail latched comparator. Hence the performance of the pre-amplifier based clocking comparator is limited by the

Vol 06, Article 06601; June 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

static power dissipation in the evaluation or regeneration phase. Due to low power consumption, high input impedance and full-swing output, dynamic latched comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. They use positive feedback mechanism with single couple of back-to-back cross coupled inverters (latch) in order to convince a low input-voltage difference to a full-scale digital level in a short time.

4. PROPOSED SYSTEM

4.1 Pre-Amplifier Based Clocked Comparator

The pre-amplifier based clocked comparator is composed of two levels as depicted in Fig. 2. The first stage is the amplification stage, which consists of the transistors M1–M4 and M9. More practically, the input-referred latch offset voltage can be shortened by applying the pre-amplifier preceding the regenerative output latch stage. It can expand a low input voltage difference to a large enough electric potential to overcome the latch offset voltage. The second phase is the regenerative stage that is comprised of the transistors M5– M8 and M10. The circle functions in two phases, namely the amplification phase and the regenerative (evaluation) phase. When the clock (CLK) is low (amplification phase), the tail transistor M9 turns ON and M10 turns OFF. When CLK is LOW, only amplification stage works. In addition, the amplification stage is designed to produce its output closer to VDD-|Vthp| which can effectively reduce the charging time. In this stage Vp-Vn is amplified and fed to regenerative stage. When the clock (CLK) is high (regeneration phase), M10 turns ON and M9 turns OFF.

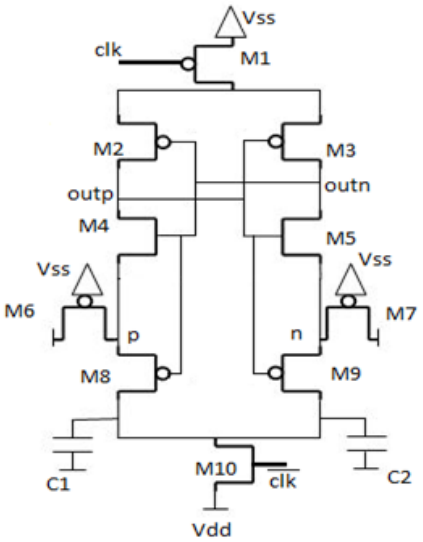

Fig. 2 Preamplifier based clocked comparator

When cock is given at M1 with supply Vss, the charging transistors M2, M3, M4, M5 drives all other transistors in the circuit. The input is applied at nodes p and n, which charges the capacitor C1 and C2. The input which is having high frequency gets discharges quickly. The discharged transistor gets charged with the supply applied at the transistors M6 and M7, which are called as floating transistors. This makes the part of the charged transistor as a closed circuit, by making the other part to be opened circuit. The final output can be obtained at the nodes outp and outn.

SIMULATION RESULTS

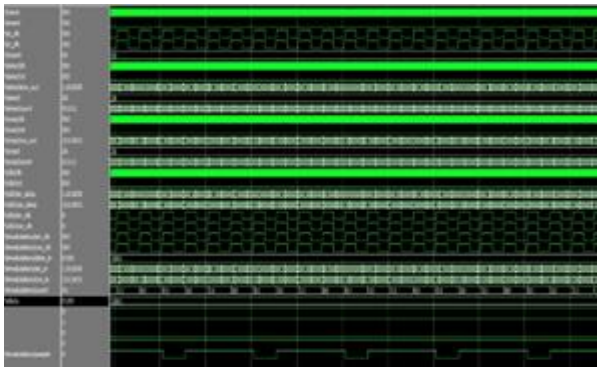

Fig. 3 Output of Double Tail Comparator

Vol 06, Article 06601; June 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

The Fig. 3 shows the output of double tail comparator. The inputs are Vp, Vn and gate. The output is out_min and out_max.

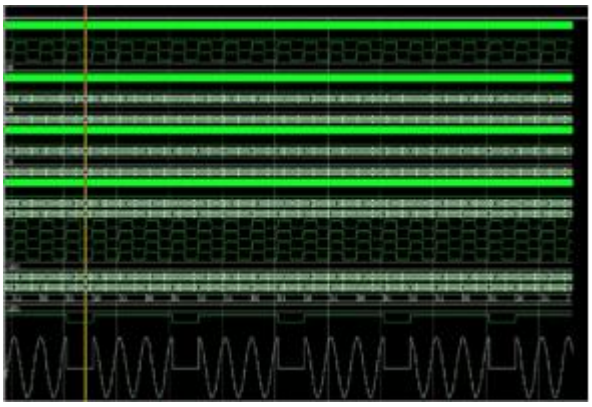

Fig. 4 Output of Pre-Amplifier based Comparator

The Fig. 4 shows the output of Pre-amplifier based clocked comparator. The inputs are Vp, Vn and gate. The output is out_min and out_max.

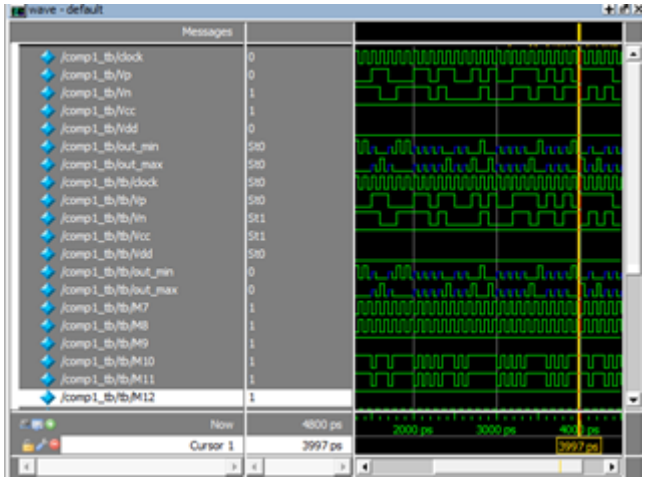

Fig. 5 Output with Glitches

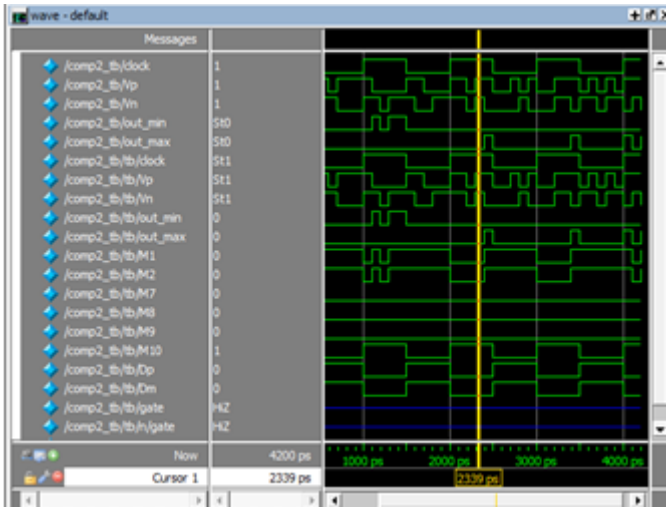

Fig. 6 Glitch free Pre-Amplifier based Comparator

The Fig. 5 shows the simulation result of comparator with glitches which affects the accuracy of the result; the blue colored wave represents the presence of glitches and the simulation of glitch free comparator shown in Fig. 6 which is based on the pre-amplifier based comparator.

Vol 06, Article 06601; June 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

Table1. Power Consumption

Parameters	Existing system	Proposed system
Number of pins	7	5
Core dynamic power	0.14mW	0.0mW
Core static power	46.12mW	46.11mW
I/O thermal power dissipation	13.94mW	9.34mW
Power	60.2mW	55.25mW

The above table indicates the power comparison of the existing and proposed system in which the existing system has the total power consumption of 60.2mW and the proposed is 55.25mW. The above table lists the power analysis of both existing and projected systems. The consumption of dynamic and static power are diminished when compared with the existing method. The power efficiency is increased to 12% than the existing scheme.

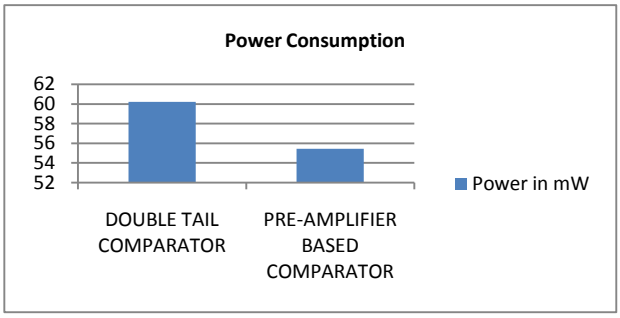

Fig. 7 Power analysis of Existing and Proposed system

The graph represented above shows the power analysis of the existing and proposed system. The power efficiency so obtained is 12% greater than the existing system.

5. CONCLUSION

This paper presents the pre-amplification process for low power applications. Therefore, this technique can be applied to all types of applications which requires low power. The area is reduced by the number of logical elements in it. Since the area gets reduced, the processing time lag between the transistors also gets diluted. When compared with the conventional techniques of the comparator, this pre-amplification technique greatly improves the power efficiency to 12%. This process can be implemented in the parallel prefix structure based comparator that is used to compare the most significant bit, which is used to compare in the bitwise order towards the least significant bit only when the comparison bits are equal.

REFERENCES

[1] Pedro M. Figueiredo (2007), *Member, IEEE*, and João C. Vital, *Member, IEEE*, Kickback Noise Reduction Techniques for CMOS Latched Comparators, VOL. 53, NO. 7.
[2] Suat U. Ay(2010), A sub-1 Volt 10-bit supply boosted SAR ADC design in standard CMOS.
[3] Mr. Deepak Joseph Babu, Mr. Sunil Jacob,(2014) Design of a Low Voltage low Power Double tail comparator in 180nm cmos Technology.
[4] Bernhard Goll and Horst Zimmermann (2009), A Comparator With Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65 V, , VOL. 56, NO. 11.
[5] Masaya Miyahara, Yusuke Asada, Daehwa Paik and Akira Matsuzawa (2009), A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs.
[6] Ali Mesgarani, Mustafa N. Alam, Fan. Z. Nelson, Suat U. Ay (2009), Supply Boosting Technique for Designing Very Low-Voltage Mixed-Signal Circuits in Standard CMOS.
[7] B. J. Blalock, (2000) "Body-driving as a Low-Voltage Analog Design Technique for CMOS technology," in Proc. IEEE Southwest Symp. Mixed-Signal Design, pp. 113–118.

Vol 06, Article 06601; June 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

[8] B. Goll and H. Zimmermann,(2007) "A 0.12 μm CMOS comparator requiring 0.5V at 600MHz and 1.5V at 6 GHz," in Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers, pp. 316–317.
[9] D. Shinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta,(2007) "A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold time," in Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers, pp. 314–315.
[10] A. Nikoozadeh and B. Murmann (2006), "An analysis of latched comparator offset due to load capacitor mismatch," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 12, pp. 1398–1402.
[11] J. He, S. Zhan, D. Chen, and R. J. Geiger (2009), "Analyses of static and dynamic random offset voltages in dynamic comparators," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 5, pp. 911–919.
[12] S. Babayan-Mashhadi and R. Lotfi (2012), "An offset cancellation technique for comparators using body-voltage trimming," Int. J. Analog Integr. Circuits Signal Process., vol. 73, no. 3, pp. 673–682.
[13] Osvath, P. ; High-Voltage Eng. Dept., Swiss Federal Inst. Of Technol., Zurich, Switzerland; Widmer, S. (2013), A high-voltage, high-precision self-balancing capacitance and dissipation factor-measuring bridge, Instrumentation and Measurement, IEEE Transactions on (Volume:IM-35, Issue: 1) Page (s): 19 – 23.
[14] Hyung-MinLee: GT Bionics Lab., Georgia Inst. Of Technol., Atlanta, GA, USA; Ghovanloo (2011), M., An Integrated Power-Efficient Active Rectifier With Offset controlled High-Speed Comparators for Inductively Powered Applications, Circuits and systems I:Regular papers, IEEE Transactions on (Volume:58, Issue:8), page (s): 1719-1760.
[15] He Xiaobing; Nat. Inst. Of Metrol, Beijing, China ; Wang Wei; Zhang Xin; Dai Dongxue (2013), Instrumentation and Measurement, Research on High Accuracy Current Comparator and Self Calibration Methods, IEEE Transactions on (Volume 62, Issue:6), page (s):1669 – 1674.