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Optimization and Simulation of Two Stage Operational Amplifier using 180nm Technology

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ABSTRACT

As the CMOS process entering the nanometer scale analog circuit will need to operate in lower and lower supply voltage. This trend is primarily driven by the need to low power and low voltage requirement on the consumer electronics market. With the continuous growing trend towards the reduced supply voltage and transistor channel length, designing of high performance analog integrated circuits such as operational amplifier in CMOS (complementary metal oxide semiconductor) technology becomes more critical. In this paper the two stage CMOS Operational amplifier (op-amp) has been designed using miller compensation technique which operates at 2.5V. Miller compensation technique has been employed using single miller compensation capacitor in series with nulling resistor. To achieve increased phase margin which indicate stability of a system, new design has been proposed with the help of second approach. The simulation was performed using TSMC 180nm CMOS process and design has been carried out in tanner EDA tool.

Keywords*: CMOS, Phase margin, Two stage CMOS operational amplifier, Tanner EDA Tool*

[1] INTRODUCTION

Operational amplifier is among the most used electronic devices today, used in a wide range of consumer devices, industrial and scientific. In many applications of operational amplifiers, the gain of a single stage amplifier is not sufficient. Architectures of operational amplifiers using two or more gain stages widely used in higher gains are needed. Op-amps are available in many topologies, a two stage op-amp is an example of this kind, which is used when the high input impedance and low output impedance is needed. CMOS operational amplifiers can be used effectively for the practical consequences for example the design of a switched capacitor filter, analog-digital converters, oscillator, and digital-analog converter and waveform generators.

Operational amplifiers are used as a basic building block in many analog and mixed signal systems. During designing of op-amp various electrical characteristics such as gain, offset, phase margin, unity gain bandwidth etc. all have taken into consideration. To meet the desired specification better compensation strategy and topology has to be selected. Among various introduced topologies, here we have chosen up two stage op-amp topology for high input impedance and low output impedance. The first stage provides high gain and second stage provides large output swing. In various op-amp applications, gain with single stage is not sufficient. To achieve higher gain more stages have to be introduced which provides additional phase shift to the system. For Closed loop circuit stability and well maintained magnitude and time response, frequency compensation is needed. The important feature of compensation technique is that they can increase the phase margin. The realization of a CMOS op-amp that combines an acceptable gain with high unity gain frequency has been a difficult problem.

The objective of this paper is to perform a comparative analysis between two stage CMOS op-amp and two stage CMOS op-amp using compensation capacitor along with nulling resistor effect . Design has been carried out in tanner EDA tool along with simulation results by TSMC 180nm CMOS technology.

2. BLOCK DIAGRAM OF TWO STAGE CMOS OP-AMP

Operational amplifier is the backbone for many analog circuit designs. Optimization of all parameters in a design has become mandatory now-a-days. In the recent years, various topologies of a new genus have evolved and been used in various applications. Here, we chose a simple pair differential amplifier Immune input amplifier, common source amplifier (high gain) to the output amplifier, a current mirror circuit as bias circuit, and a buffer circuit compensation current as well as a Miller capacitance in series with one another.

The topology of the circuit designed is that of a standard CMOS two stage op-amp. It comprised of three subsections of circuits, namely differential gain stage, second gain stage and bias strings. The topology used for two stage CMOS op-amp is shown in figure 1. The circuit consist of 8 transistors out of those 5 are NMOS and remaining 3 are PMOS transistors. The transistors named from M1 to M4 are showing the differential transconductance first stage of the circuit. The M1 and M2 are the N-channel MOSFET transistors forming the input stage to the op-amp circuit. The current mirror configuration comprised of M3 and M4 used as a active load for input differential stage. Second stage uses current sink load inverter where M6 acts as driver and M7

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works as load. The output from drain of M2 will be amplified using current source configuration represented by M6. The biasing in a circuit is achieved using two transistors M5 and M8 and a current source. The compensation capacitor is shown by CC and the load capacitor is represented by CL.

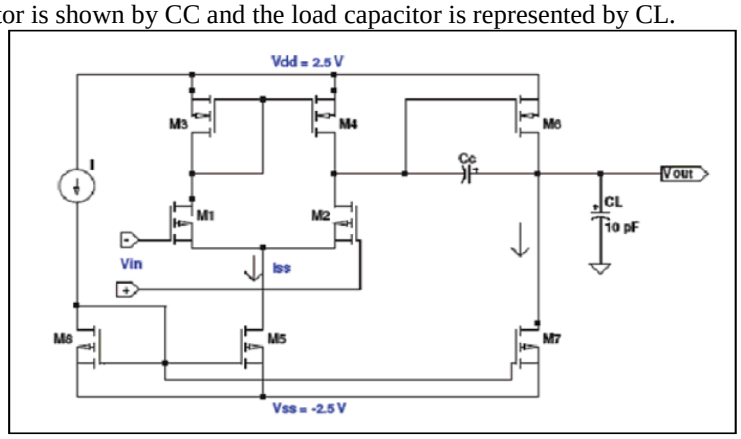

Fig.1. Topology Used for Two Stage CMOS op-amp

2.1 AC ANALYSIS

In AC analysis, an ac signal is applied to both the terminals of the input stage. The schematic for two stage CMOS op-amp is shown in figure 2. It is considered that all MOS transistors are operating in saturation region.

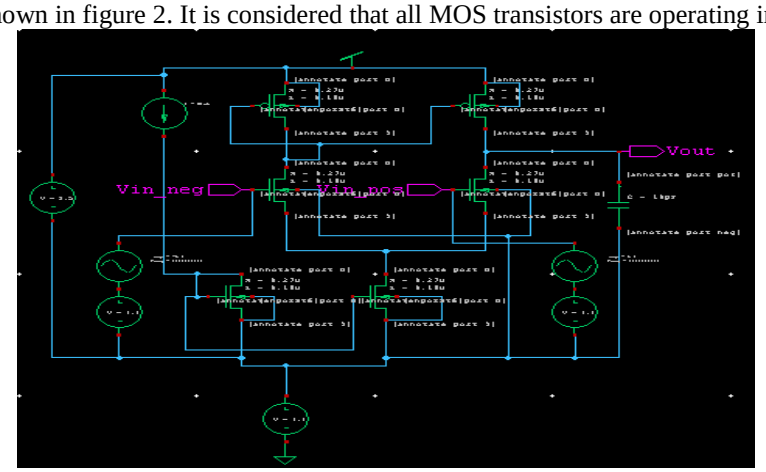

Fig.2. Topology Used for Two Stage CMOS op-amp

Table 1. Specifications CMOS op-amp for two stage

Specification Name	Value
Supply Voltage	2.5
Bias Current	30uA
Load Capacitor	10pf

2.1.1 Simulation Results

Gain and Frequency Response for Two Stage CMOS op-amp is shown in figure 3.

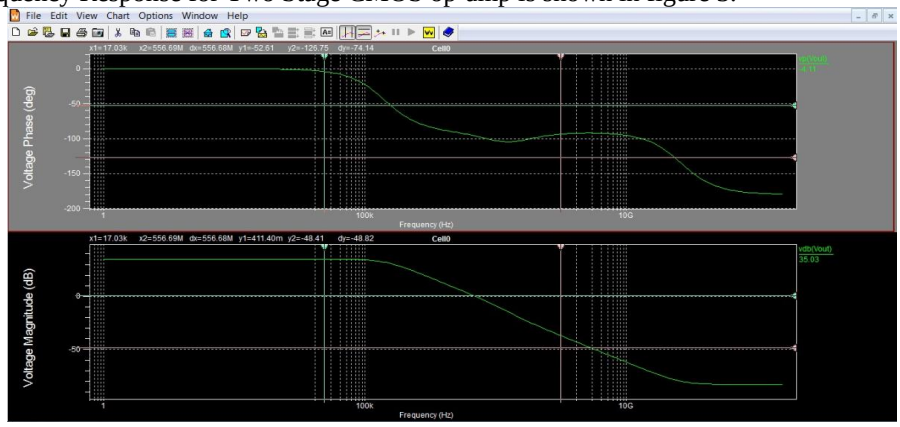

Fig.3. Frequency Response for Two Stage CMOS op-amp

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2.1.2 Analysis Output

With the help of AC analysis we can estimate several performance parameters like gain, unity gain bandwidth, -3dB bandwidth, phase margin etc.

Table 2. AC Analysis Parameters for Two Stage CMOS op-amp

Parameter Name	Parameter Value
Gain Margin	75 db
Phase Margin	80 degrees

3. TWO STAGE CMOS OP-AMP WITH COMPENSATION STRATEGY

The schematic for unbuffered two stage CMOS op-amp with single capacitor miller compensation (SCMC) with nulling resistor for 180nm technology is represented in figure 4. It is considered that all MOS transistors are operating in saturation region. The MOS transistors aspect ratio variations affect the performance of the two stage CMOS op-amp. Therefore the aspect ratio has to be selected properly to optimise the performance of the circuit. The single capacitor miller compensation strategy has a drawback which is eliminated with the help of single capacitor in series with nulling resistor miller compensation strategy. The compensating capacitor is attached to provide compensation.

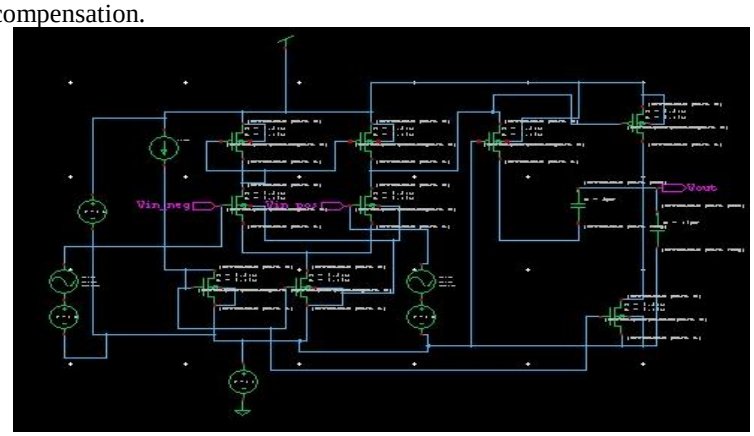

Fig.4. Two Stage CMOS op-amp Using SCMC with Nulling Resistor

3.1 AC ANALYSIS

In AC analysis, an ac signal is applied to both the terminals of input stage. With the help of AC analysis we can estimate several performance parameters like gain, unity gain bandwidth, phase margin etc.

Table 3. AC Analysis Output for Two Stage CMOS op-amp Using SCMC with Nulling Resistor

Parameter Name	Parameter Value
Gain Margin	81 db
Phase Margin	85 degrees
3dB Bandwidth	115KHz

3.1.1 Simulation Results

Gain and Frequency Response of Two Stage CMOS op-amp is shown in figure 5.

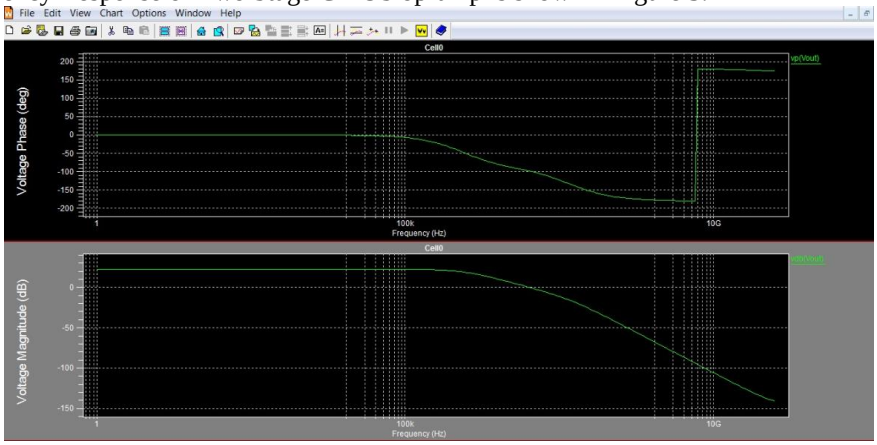

Fig.5. Frequency Response for Two Stage CMOS op-amp Using SCMC with Nulling Resistor

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4. CONCLUSIONS

The future implications of the project are very wide since Op-amp is a device which is now a days using in many applications. In order to achieve optimized performance devices are scaled down accordingly.. Along with negative feedback configuration addition of each stage in multistage op-amps introduces another pole in the system which creates stability problem. For this reason, a miller compensation technique has been employed in system. In this paper two stage CMOS op-amp with miller compensation technique has been designed and simulated at 180nm technology. Two Stage CMOS op-amp Using SCMC with Nulling Resistor increase the phase margin, which indirectly makes system more stable, miller compensation capacitor is used in series with nulling resistor, which provides gain of 91dB and phase margin of 85 degree. We can further work on lots of researches in this field in which we can try to improve all the parameters further by utilizing the advantage of both the previous research results and can study further to enhance the capacity
and efficiency of Operational amplifier. So it can play more important and advantageous role in electronics.

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