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Area-Efficient Low Power OTA-C Filter for Biomedical Applications

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ABSTRACT

The paper presents a sub-Hertz low power OTA-C filter intended for signal smoothening applications in portable medical devices. In this paper, operational trans-conductance amplifier is designed using a feedback mechanism .Advanced compact based model is being implemented to achieve low trans-conductance and hence low power. A self-biased current source of 200pA/1nA is generated using the concept of inversion level. The intended design achieves low frequency in the range of 61mHz-64 Hz by incorporating non-overlapping switches with varying duty cycle. The circuit has been implemented in Cadence 90nm (gpdk) technology with a supply of 1V.It achieves a power of approximately 5nW.Area consumption is also feasible for the design. Area has been reported to be 0.0014mm^2.

Keywords: *Feedback Filter, Low power, Switches, Bias Current, Inversion Region*

1. INTRODUCTION

In biomedical equipment and sensors, low frequency types of filters have been extensively used [1]. Slow rate phenomena like pressure, chemical concentration, flow rate and temperature are sensed by sensors. For this purpose, intended filters are used in the form of anti-aliasing filters, gain controllers and also in the isolation of required signal. Biomedical signals [2] are in the range of 10mHz-100Hz. Sub-Hertz filters are used to smoothen the signal before further processing. Here, the designed filter is a part of wearable breathing detector [3]. Signal is conditioned with the aid of Sub-Hertz frequency filters and is further subjected to processing blocks.

Despite its practicality, the problem of designing large time constant is a challenging task. Such requirement needs switched capacitor [4] designs with large valued capacitors and subsequently high power for lower ON resistance. In g_m-C based topology, the 3-dB frequency is determined by g_m/C. The capacitance value is limited to 50pF due to restriction in Silicon area. Small value of trans-conductance leads to increase in noise level. In order to solve the issue of desired constraints, various techniques have been reported. Floating gates have added to input transistors to attenuate the effective signal voltage but it increases the noise level. With this technique, El. Mourabit et.al [5] achieved a cut-off frequency of 500mHz. El. Mourabit et.al [5] and Veeravalli et.al [6] utilized the transistors operating in triode region for converting voltage into current. Veeravalli et.al [6] used feedback mechanism and reported a cut-off frequency of 1.5Hz.

Bulk transistors have been used to reduce bulk trans-conductance. This achieved a170mHz of cut-off frequency but it reduced input impedance as well. With the help of current division technique, 53mHz was reported as the cut-off frequency. In this technique, current splitters were implemented to lower output current from the trans-conductor, and this has reduced the effective trans-conductance, but it increases circuit area. Current cancellation technique has also been used where current is lowered by adding input transistors with its drain terminals cross connected. Cascaded form of trans-conductance amplifiers and trans-resistance amplifiers, each having different value, so as to reduce overall trans-conductance. This has achieved 100mHz cut-off for the integrator. It showed poor performance because every section adds to noise and distortion. The clock and bias current is generated using HP8112A and Keithley236 respectively [7].

A new topology of low pass filter is based on a combination of an OTA-C filter and switch controlled capacitor. A trans-conductor with the help of switches lowers the value of trans-conductance element in OTA-C filter. Varying the duty cycle of clock makes the cut-off frequency of designed filter tunable as well as controllable. Biasing of the circuit is performed at the level of pA/nA so as to make the trans-conductance operate in sub-threshold region. This will reduce the current and hence trans-conductance effectively. Biased source has self-biased characteristics which are being implemented by using self-biased current source (SBCS) circuits. This gives satisfactory performance in low power operation. The SBCS being employed here is having desirable features, namely 1) Mosfets are biased in sub-threshold region as well as moderate inversion. 2) The current at the output is in proportion with Mosfet's specific current. Section 2 gives details about the principle of new topology. In section 3, the implementation of OTA has been described. Section 4 gives design methodology of self-biased current source. Section 5 represents simulation results. In section 6, conclusions are drawn based on the results.

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2. PRINCIPLE OF OTA-C TOPOLOGY

In Figure 1, basic symbol of OTA has been presented. It is a trans-conductor based element in which output current is being controlled by input voltage. An OTA device is represented by equation I.

$I_o=g_m (V_{in+} - V_{in-})$…….. (I)

The advantages of OTA are described as follows:

- By varying bias current, g_m value can be adjusted.
- Matching between amplifiers.
- Trans-conductance varies linearly with bias current.
- High valued Signal to Noise ratio.
- Simple in design.
- Less number of components are required.

Most of OTA structures are integrators with an OTA and a capacitor. The trans-conductance of OTA is given by equation II.

$g_m = I/2V_t$…….. (II)

Here, V_t is the thermal voltage and I is the bias current. If the bias current is changed, trans-conductance value will change accordingly. With the inclusion of feedback, the filter characteristics can be made independent of gain.

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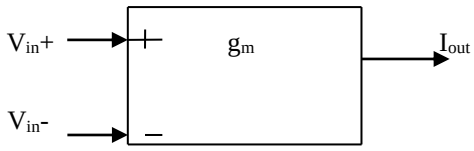

Figure 1: Basic OTA Symbol

Fig.2 describes the operation of a complete low pass filter. A trans-conductor output is clocked and is placed with feedback mechanism along with capacitor to form a first order low pass filter and a switch is included between capacitor and output of the structure. The current I_1 flows into capacitor at the time when switch SW_1 is closed. The total current at the output, I_2 is reduced by a factor of δ, where δ is the duty cycle of switch SW_1. Average current of the structure, I_2 is given by $I_2= \delta$ X I_1. The g_m of the trans-conductor decreases in the same proportion. On time axis, lowering of trans-conductance occurs.

This operation is controlled via switches. The cut-off frequency f_c as well as trans-conductance are digitally controlled using switches SW_1 and SW_2. For a first order OTA-C type of filter, its time constant is mentioned by equation III.

$\tau = C/ g_o + g_m$…….. (III)

Where g_o represents the output conductance. In order to make time constant adjustable, the term g_m must dominate over g_o. When switch is kept open, the voltage at the capacitor node is not intervened since they become isolated. The value of g_o is considered at the time when switch is closed. Hence, g_o scales in same proportion as g_m does. This makes g_m a dominance factor in the absence of duty cycle. Therefore, no extra circuit is required to lower the value of g_m. There arises a problem in the presence of one switch since opening of switch results in saturating the output of the device near V_{dd} and ground since there is no path for the current to flow.

In Figure 2, two OTA buffers are added so as to avoid this discrepancy. First buffer is fixed between the output voltage and capacitor for isolation. Another buffer is placed between capacitor and g_m output via another switch SW_2 which is in opposite phase with respect to switch SW_1. The inclusion of second buffer makes a path for current from g_m to flow, when main switch SW_1 is open. The gm output remains constant even if the current flows into capacitor or not. This prevents the output to saturate between rail voltages measures. This also decreases the charge injection effect, which usually occurs with switches. When switch SW_1 is turned ON, charge is introduced in capacitor forming low impedance. When switch SW_2 is ON, charge is implanted in the buffer present in a negative feedback arrangement.

Vol 06, Article 09635; October 2015
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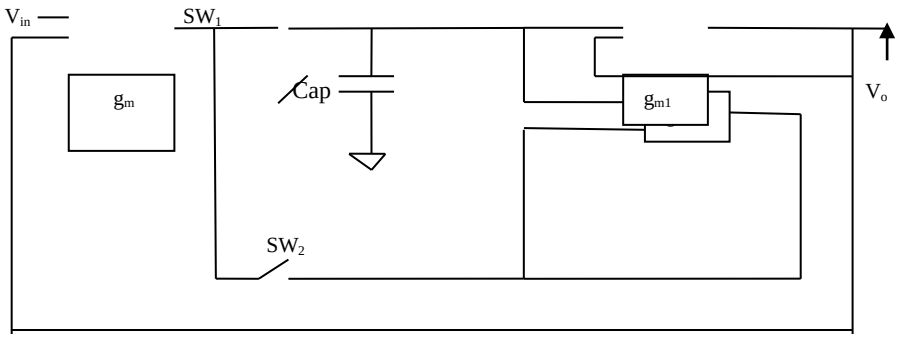

Figure 2: Complete Low Pass Filter with 1st Order OTA-C filter and Two Buffers Placed in Feedback Path with Switches to Lower Trans-conductance.

The load capacitor is the sum of capacitance of buffer and capacitance of negative feedback, thus increasing the total capacitance. The frequencies at which both switches operate are higher than filter's bandwidth so that voltage ripples are eliminated when necessary.

3. IMPLEMENTATION OF OTA-C TOPOLOGY

The trans-conductors implemented as g_m and g_{m1} are depicted in Figure 3. As shown above in Figure 3a, the trans-conductance g_m is a cross operational amplifier with its two differential pairs connected in the doublet form .The W/L ratio for input transistors are chosen to be 3:1.The bias current is set at 200pA for its nominal operation. The trans-conductor g_{m1} topology is shown in Figure 3b. It is being implemented as two identical buffers in OTA-C filter and they are placed in a feedback path. They are basically differential pairs and their outputs are fedback to negative inputs for unity gain in terms of voltage.

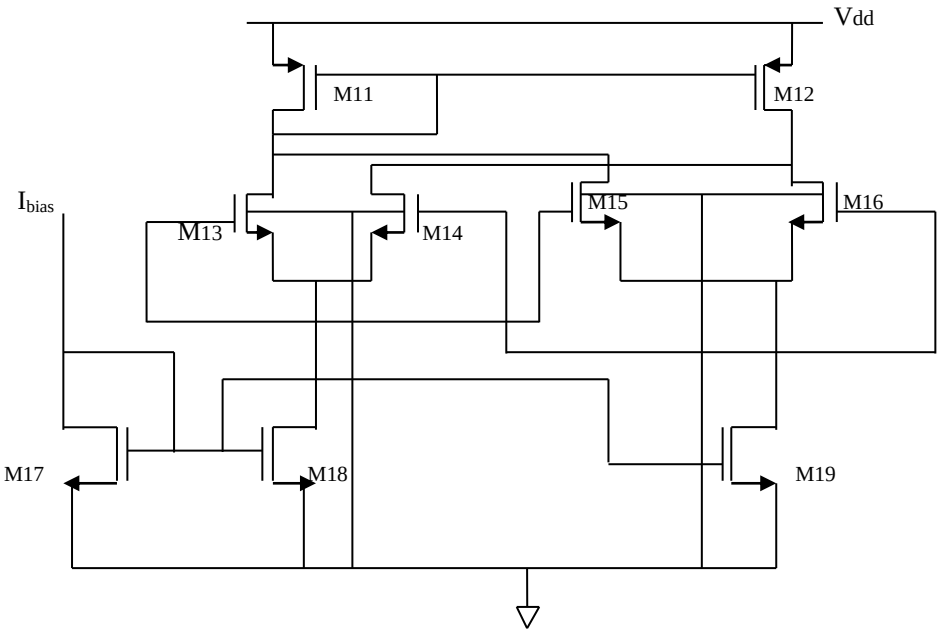

Figure 3a: Filter Trans- conductor g_m uses a Double Cross Arrangement with a 3:1 Aspect ratio. A 0.5-Vcommon-mode (CM) Signal is at Input for Correct Operation.

feedback path. They are basically differential pairs and their outputs are fedback to negative inputs for unity gain in terms of voltage. The bias current I_{bias} in buffer is set at 1nA.The inputs are fairly equal and hence has little contribution in terms of distortion in filter.

Vol 06, Article 09635; October 2015
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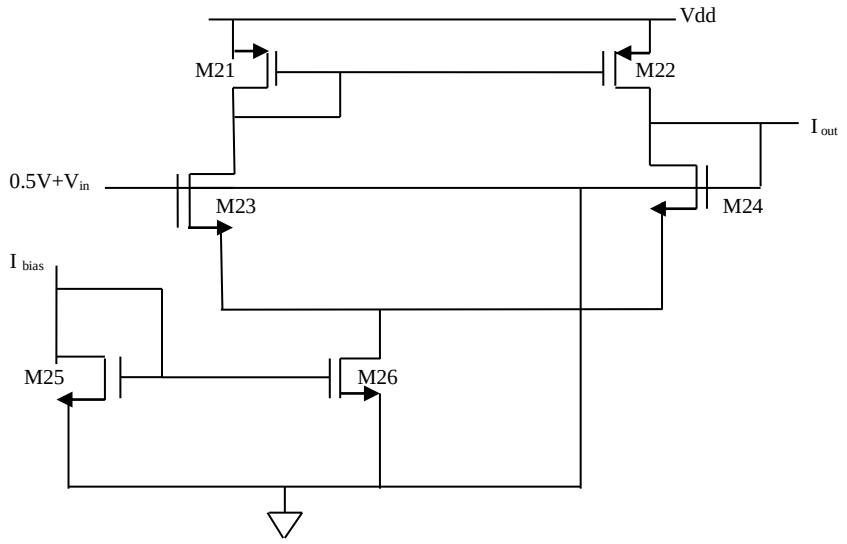

Figure 3b: Buffers g_{m1} are Differential Pairs in a Unity Gain Topology.

4. DESIGN AND METHODOLOGY OF BIAS CIRCUIT

Current references are important blocks for the purpose of biasing of analog circuits. A design methodology is based on the concept of levels of inversion. A self-biased current source circuit is operated at nominal inversion level.

4.1 ADVANCED COMPACT MODEL

Advanced Compact Model (ACM) model is basically a current based Mosfet model which implements the idea of inversion level. As the ACM model suggests, the drain current I_D is divided into the forward and reverse currents as shown in equations IV-VI.

$I_D=I_F-I_R=I_S\ (i_f-i_r)$…… (IV)

$I_S=I_S(W/L)=S.I_{SQ}$…….. (V)

$I_{SQ}=\mu.\ C_{ox}\ .\eta.\Phi t^2$…… (VI)

Here, I_F and I_R are termed as forward and reverse currents. When Mosfet is in state of forward saturation, then $I_F >> I_R$ and therefore $I_D = I_S\ i_f$. Here, I_S is called specific current and sheet specific current is denoted by I_{SQ}. Respectively, forward and reverse inversion levels are denoted as i_f and i_r .Φt, Cox, μ, η and S=W/L are termed as oxide capacitance per unit area, mobility thermal voltage, slope factor and aspect ratio of transistor respectively.

The Self Cascode Mosfet (SCM) is the basis of SBCS as depicted in Figure 4.If reference current I_{ref} is exact copy of specific current, then it acts as voltage generator and vice–versa. The voltage of the circuit reference is generated using SCM (M3, M4) that is being biased in weak inversion. Voltage-current conversion is implemented applying SCM (M1, M2) and this is biased in moderate inversion. Mosfets namely M6-M9 establishes self -biased voltage following current mirror which applies the voltage to node V_x of M3-M4.The PMOS (M5-M10) devices are current mirrors of unity gain. Trapezoidal Mosfets are used in PMOS mirrors so as to facilitate in the regulation of current reference. This saves silicon area and still efficient to operate at low voltage.

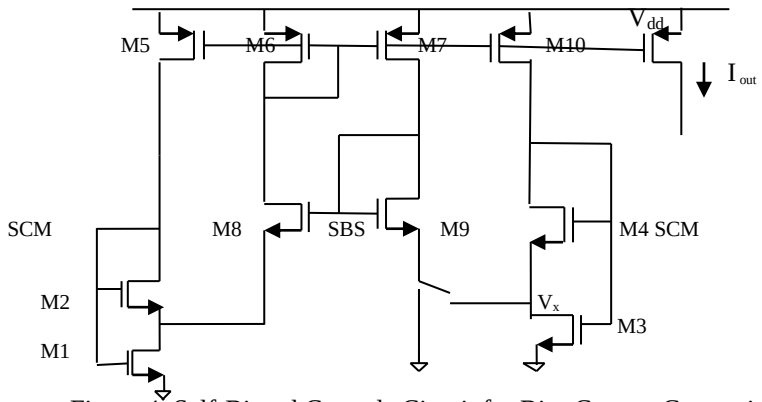

Figure 4: Self-Biased Cascode Circuit for Bias Current Generation.

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http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
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5. SIMULATION RESULTS AND COMPARISON

Presented topology of a low pass type filter has been implemented in Cadence 90nm (gpdk) CMOS technology at nominal supply voltage of 1V.

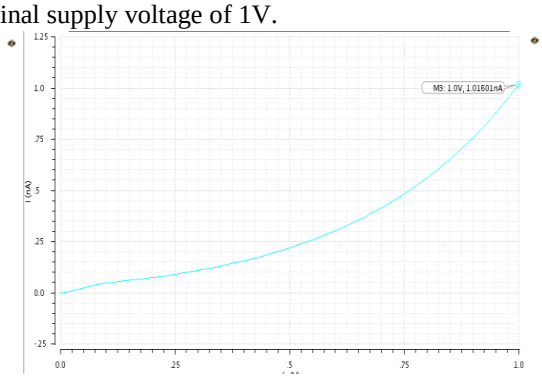

Figure 5: Bias Current of 200pA.

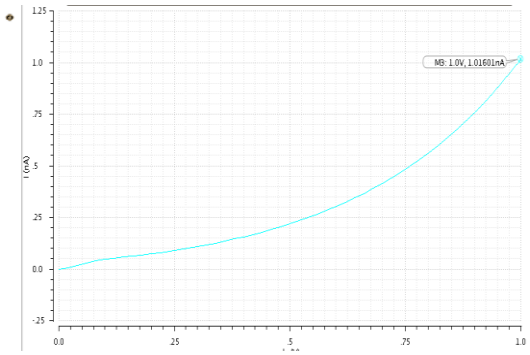

Figure 6: Bias Current of 1nA.

Figure 5 and Figure 6 are the bias currents generated from the self-biasing cascode circuit with trapezoidal Mosfets to provide satisfactory results while being operated at low voltage and hence gives low power consumption. The frequency response was measured by changing duty cycle of the clock and varying the bias current. Tunable frequencies were obtained as shown in Figure 7 and Figure 8 with the duty cycle of .00025% and .025% respectively.

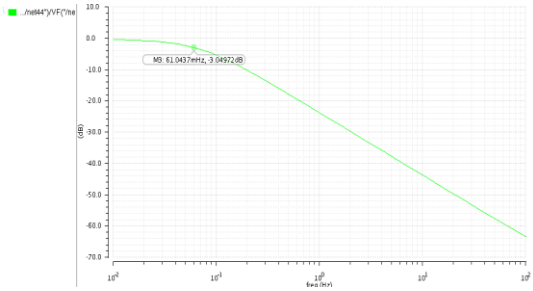

Figure 7: Cut-off Frequency at Clock Frequency =1 kHz, Duty cycle=.0025%, Fc=61mHz.

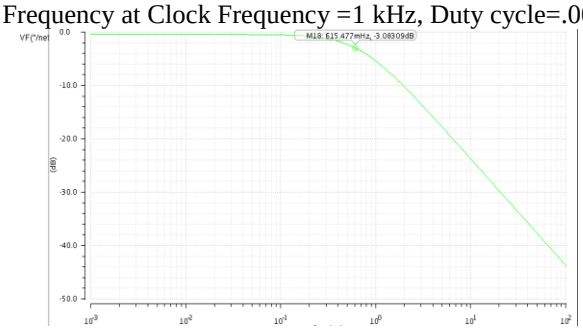

Figure 8: Cut-off Frequency at Clock Frequency =1 kHz, Duty Cycle=.025%, Fc=615mHz.

By increasing the duty cycle to 40% and setting the clock frequency equal to 20 kHz, a frequency of 64Hz is obtained. This type of topology is very suitable and desirable in various biomedical applications. Table 1 represents the comparison and performance in terms of power, area and frequency. Figure 9 represents the layout of proposed filter.

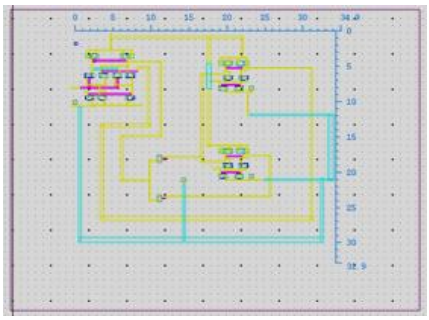

Figure 9: Layout of Proposed Filter

Vol 06, Article 09635; October 2015
http://ijves.com
International Journal of VLSI and Embedded Systems-IJVES
ISSN: 2249 – 6556

Table1. Circuit Performance of Proposed Low Pass Filter

Parameters	Proposed work
CMOS process technology	90nm
Vdd	1V
Current	5nA
Power supply	5nW
Area	.0014mm^2
Cut off range	60mHz-64Hz
Capacitance	2pF
I_{bias}	200pA/1nA

6. CONCLUSIONS

An ultra-low frequency scaled down to milli-Hertz cut-offs, and a topology of low pass filter is being implemented. This proves to have excellent characteristics when compared with the previous literature work till date. An external bias circuit is designed using the concept of ACM model The operation is carried by implementing a switch at the output node of trans-conductor so as to decrement the trans-conductance of OTA-C filter. The supply voltage is 1V for the filter and bias circuits. Measured results have led to reduction in area which came out to be .0014mm^2.The power is obtained in terms of nano-watts. The frequency is satisfying the concerned application and is tunable in nature, varying from 61mHz -64Hz. While excluding the bias current generation and switch, the overall power of the circuit drawn from the supply is approximately 5nW.

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