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VLSI IMPLEMENTATION OF 12-BIT SAR ADC OPTIMIZING DYNAMIC POWER

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ABSTRACT

Autonomous acoustic-sensor nodes rely on low power circuit techniques to enable energy harvesting as a means of sustaining long-term, maintenance free operation. This work pursues the design of a low-power analog to digital converter (ADC). The proposed ADC has a sampling rate of 0-100kS/s and a resolution of 12bits. Based on conventional successive approximation ADC architecture which is suitable for low power operation, a new faster and energy efficient solution is presented. The input structure of the new solution consists of transmission gates and capacitors only and there is no active element included. This approach eliminates the buffer used in the common mode path. This together with a technique of self timed comparator approach, the power consumption is noticeably reduced, while at the same time the sampling rate is increased. Integrated capacitors are laid-out in a new common-centroid manner that minimizes edge effects. This helped in reducing the unit cap value for the required matching and it not only adds up in the area saving but also in the power delay product improvement.The ADC has been simulated in 0.18um technology. All circuits are powered using a 1.8 V supply. At a resolution of 12- bits, and a sampling rate of 100 KS/s, the power consumption of the entire ADC core is 80 uW.

Keywords: *analog to digital converter (ADC), proposed ADC, Conventional ADC, Self timed comparator, lowpower*

1. INTRODUCTION

Autonomous wireless sensor networks have received a lot of attention recently by various sectors of the research community. Although protocols and requirement specifications are still being defined at the communication, network architecture, node architecture, and circuit levels, design constraints and applications are already emerging. The vision of a micro-sensor network includes dense, intelligent nodes that are energy-autonomous and that operate in an ad-hoc manner. Such networks have diverse applications ranging from military surveillance, reconnaissance, and damage assessment to environmental forest fire detection and industrial process monitoring. The design of micro-sensor node hardware is constrained by several factors, many of which can be derived from collective considerations of the target applications. To be energy-autonomous, nodes must be powered entirely by an energy-harvesting source. This places demanding, low-energy requirements on the constituent circuits. Ad-hoc deployment and operation requires that nodes be fault tolerant and able to adapt to unpredictable environments and network characteristics. Finally, high density and ubiquity places a cost constraint on nodes, reducing their acceptable price per unit to a few cents.

This work focuses on the development of a low power ADC suitable for sensor network nodes. Although design specifications and optimizations will be undertaken with this application in mind, the circuit techniques developed, and indeed the final ADC, will be useful for a variety of low power systems.

2. CONVENTIONAL ADC ARCHITECTURE

The ADC architecture of the fully differential successive approximation switched capacitor ADC which was used so far consists of two capacitor arrays, two blocking capacitors, a fully differential buffer, a fully differential comparator with offset cancellation, a successive approximation register (SAR), and a control logic [1], [2]. Various possible structures to realize the track-and-hold function exist [3], [4]. In this solution, the whole capacitor array is used as a track-and-hold stage and as a DAC (Maindac) to perform the successive approximation. To increase the resolution and to avoid a large capacitor array another DAC (Subdac) is used, which interpolates the least significant bit of the capacitive Maindac and may be either resistive or capacitive.

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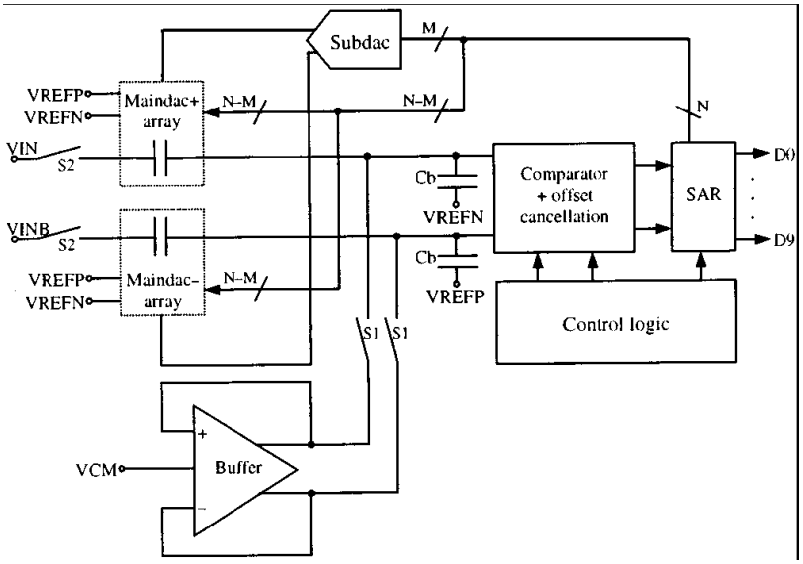

Fig. 1. Conventional ADC architecture

Fig. 1 shows the block diagram of an 10-bit converter, which comprises a 6– bit Maindac and a 4 -bit resistive Subdac. The whole conversion is divided into two parts, as shown in Fig. 2. The first part is the tracking phase, in which the bottom side of the capacitor array is connected to the input voltage of the ADC and the differential buffer forces the top side of the capacitor arrays to the common mode voltage VCM.

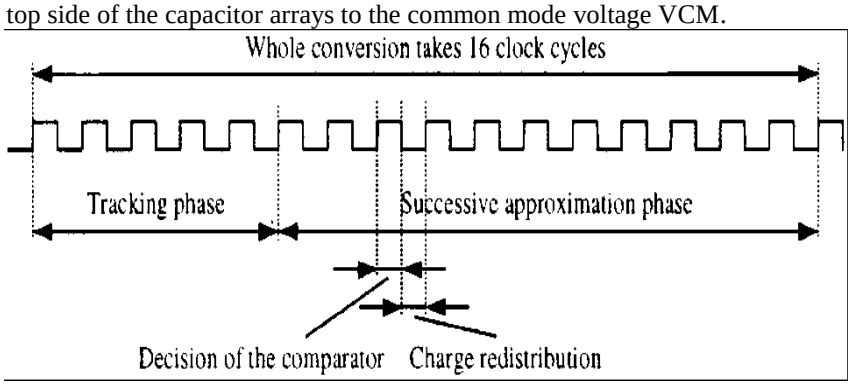

Fig. 2. Timing of the conventional ADC.

This is necessary for storing the differential input voltage VIN–VINB in the capacitor arrays and providing a well defined starting point for the successive approximation. The differential buffer must have enough gain at Nyquist frequency to hold the topside of the capacitor array to at least 10 bit accuracy for an 10bit converter. Furthermore, the buffer must settle to bit within the tracking phase. To fulfill both requirements a wide-band amplifier is used. This causes a large current consumption to obtain 10-bit resolution at 100 kS/s; even more current is needed for a 12-bit converter.

To avoid charge loss due to overshoots or undershoots, large blocking capacitors, signed as Cb in Fig. 1, at the input of the comparator are necessary especially when using the converter in single-ended mode. Fig. 3 illustrates the possible wide variation of the critical output signals of the two Maindacs, which is reduced by the large blocking capacitors. These additional capacitors increase the input and reference capacitance of the ADC. For a 12-bit converter, the input and reference capacitance is four times larger than that for a 10-bit converter. In most applications, an on-chip buffer is used to provide the input signal to the ADC, but with such a large input capacitance, it is very hard to achieve more than 250 kHz with 12-bit accuracy in an integrated system. During the tracking phase, the offset cancellation is performed. In this phase, the common-mode input voltage of the comparator depends on the voltage VCM, which is derived from the reference voltage. During the successive approximation phase the common mode input voltage of the comparator depends on the common mode voltage of the input signal. So the operating point of the comparator during the offset cancellation is different to that at a critical decision. This difference can be up to one quarter of the supply voltage and might cause a gain error or INL error due to an insufficient common-mode rejection ratio (CMRR) of the comparator. Fig. 3 illustrates the variation of the operating point for two different input voltages in single ended mode. In both cases the input VINB is connected to the VCM voltage. In Fig. 3, the conversion of the maximum negative voltage difference at the input, which corresponds to the digital output code 0, is shown on the top whereas the maximum positive voltage difference, which is converted to

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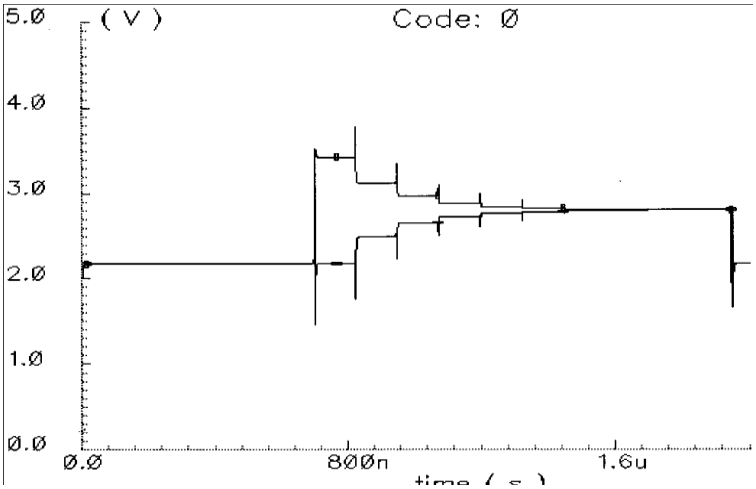

Fig. 3. Input voltages of the comparator.

the digital output code 1023. Another problem is the reduction of the input voltage swing at the comparator input due to the voltage divider built by the blocking capacitors. The swing is reduced to one quarter of the supply voltage, which decreases the signal to noise ratio of the whole converter. The second part of the conversion is the successive approximation phase, which takes clock cycles. Normally, a synchronous logic is used to activate the latch at one edge of the clock and to start the charge redistribution at the other one. The partitioning of the two clock phases can only be controlled by the duty cycle of the clock. Unfortunately, in most applications it is not possible to distort the clock duty cycle. This limits the settling time of the DACs and the comparator stage to half a clock cycle. Due to the limitations of the buffer and the RC time constant of the DAC, a maximum speed of 500 kS/s can be achieved for a 10-bit ADC with this architecture.

3. NEW ADC ARCHITECTURE

3.1 Removing the differential buffer

In the new ADC architecture, switches are used instead of the differential buffer to eliminate the insufficiency in the tracking phase. This results in an ADC without any active element except the comparator, as shown in Fig. 4 and described in [5].

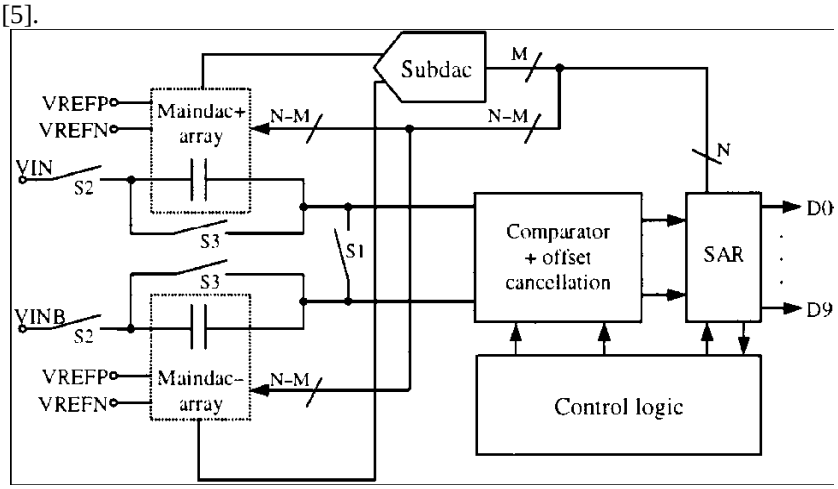

Fig. 4. New ADC architecture

A discharge phase is placed before the tracking phase, as shown in Fig. 5.

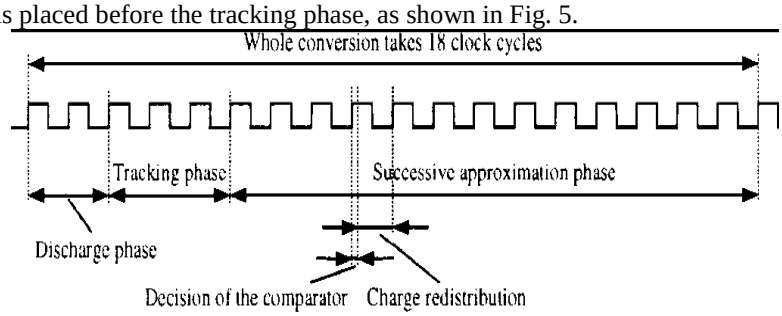

Fig. 5. Timing of the new ADC architecture

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In the discharge phase the capacitors of the two arrays are discharged by the switches S3 to have a well-defined starting point for the tracking phase. This eliminates the need for the buffer and reduces the power consumption to a minimum. During the tracking phase, the sample switch S1 and the input switches S2 are on. Both capacitor arrays are charged to (VIN–VINB)/2, even in single-ended mode. In Fig.6,the input voltages of the comparator are shown for the same setup as in Fig.3. During the whole conversion, no overshoots or undershoots are possible, even without the blocking capacitors. This eliminates the need for blocking capacitors and increases the input voltage swing of the comparator to half of the supply, which increases the signal to noise ratio of the whole converter by 2. Because of the series connection of the two capacitor arrays and the non existing blocking capacitors, it was possible to improve the resolution from 10 to 12 bit without rising the capacitive load.

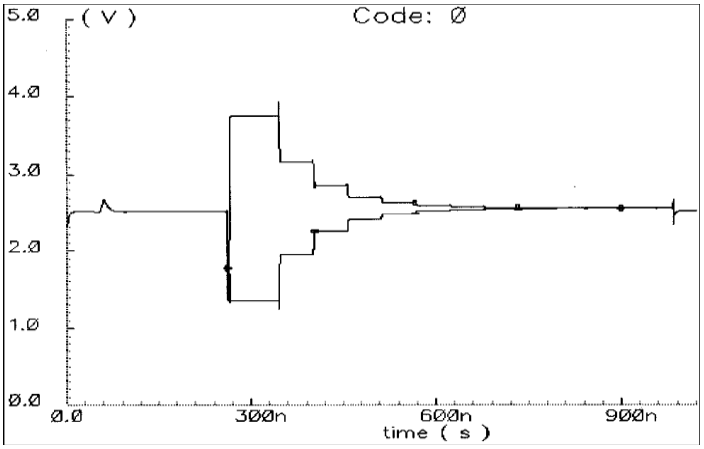

Fig. 6. Input voltages of the comparator.

This makes the implementation of an on-chip input buffer easier and allows higher frequencies for the input signal. An additional advantage is a more simplified implementation of a power-down option, because the only active component remaining has enough time to perform the power up.

3.2. Enhanced Range of the Input Voltage

For decoupling the comparator stage from the input voltage during the tracking phase, some additional switches are inserted, as shown in Fig. 7 and described in [6]. In the tracking phase, the switches S4 are off and the switches S1 and S5 are on, while in the successive approximation phase, switches S4 are on and switches S1 and S5 are off. During the tracking phase, the voltage VCM is applied to the comparator stage.

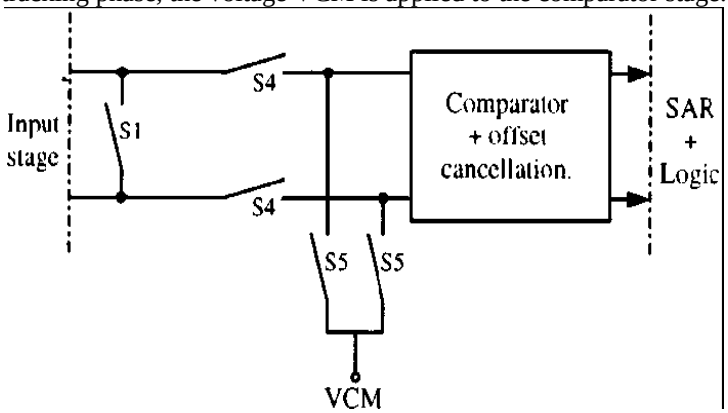

Fig.7.Decoupling of the comparator stage

The voltage VCM has to be (VREFP VREFN)/2 and can be chosen directly from the resistive Subdac, because it only has to drive the input of the comparator stage. This avoids the need for an additional buffer and means that the operating point of the comparator stage is the same during the offset cancellation as it is at all critical decisions during the successive approximation. This enables a wide variation of the common-mode input voltage and eases the design of a high-bandwidth input buffer.

3.3 Self timed comparator

Because of the improvements done so far, the remaining speed limiting part of the converter is the successive approximation itself. It is easy to implement a fast comparator, which decides within a few nanoseconds, but there is no way around the RC time constant of the charge redistribution. The relatively large capacitors are necessary to obtain enough linearity while the resistance arises from the on resistance of the transmission gates.

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The whole comparator stage consists of a fast open-loop gain stage with offset cancellation, a fast clocked comparator, and some additional logic in the SAR as well as in the control logic (see Fig. 8).

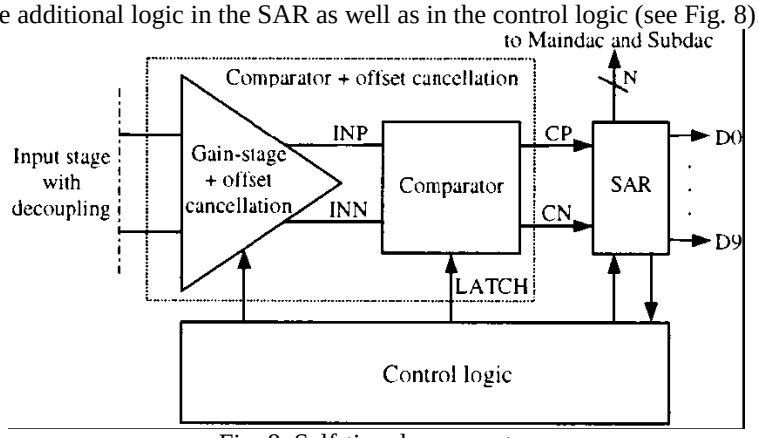

Fig. 8. Self-timed comparator

When the control signal LATCH of the comparator is low, its output signals CP and CN are set to low and its positive feedback is open. With the rising clock edge, the LATCH signal is set to high, which triggers the comparator and has the effect that one of the output signals CP or CN changes to high, depending on the input voltage difference. When the high signal is detected the LATCH signal is reset to low, the bits for the DACs are set and a new charge redistribution is started. The next rising clock edge begins this procedure a new. This increases the critical time for the charge redistribution to nearly one whole clock cycle, independent from the clock duty cycle.

The second clock edge is only used to abort a decision of the comparator if its input signal difference is too small to decide within a few nanoseconds. The successive approximation algorithm ensures that the error of a wrong decision caused by an aborted decision is always only a fraction of an LSB. This usage of the second clock edge reduces the freedom of the clock duty cycle to the range between about 25% and 75%. This self-timed solution does the time partitioning itself. When the comparator has to detect a very small voltage difference, the time for the charge redistribution is longer, because the previous one was an easy and fast decision. The subsequent charge redistribution needs less time, because an uncritical decision always follows. This correlation and the timing of the comparator are shown in Fig. 9. The combination of all those improvements makes it possible to increase the sampling rate and to reduce the power consumption at the same time.

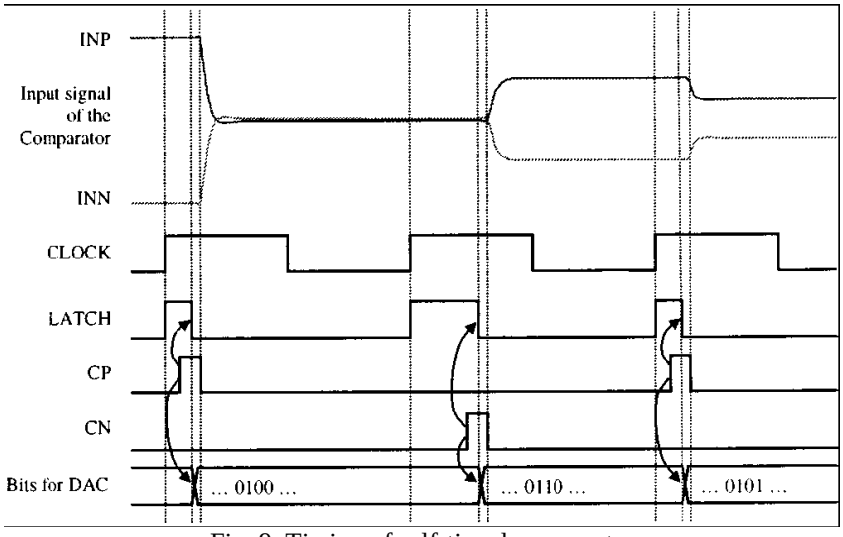

Fig. 9. Timing of self-timed comparator

4. IMPLEMENTATION AND MEASURED RESULTS

The conventional 10-bit converter which was described in Section 2 was designed in the 0.18u process of Austria Mikro Systeme Int. AG. The new architecture was implemented as a 12-bit converter in the 0.18u process as well, to compare the new architecture with the old one. Both converters are non calibrating ADCs with metal capacitor arrays. To achieve the required linearity a special common centroid layout technique was used to build a 12-bit accurate capacitor array [7], [8]. The greatest advantage of the new architecture is to have

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a higher sampling rate and lower power consumption at the same time. Furthermore the resolution is increased from 10 to 12 bit and the input and reference capacitances are almost the same for the 10-bit and the 12-bit ADC. A new input architecture of a fully differential successive approximation switched capacitor ADC has been introduced. The cancellation of the VCM buffer and the implementation of the self-timed comparator reduced the power consumption and doubled the sampling rate at the same time. 100 KS/s is guaranteed at worst-case conditions (V, temperature 125 C, worst-case process). The resolution was improved from 10-bit to 12-bit.Furthermore, the applicability of the converter in an integrated system was facilitated noticeably because of the reduction of the input and reference capacitance.

Table 1. Summary of the performance and features of the implemented ADC

Parameter	**Value**
Process	0.18u TSMC
Voltage Supply	1.8 V
Clock frequency	2 MHz
Resolution	12 bits
Maximum Sampling Rate	100 KS/s
Maximum Power consumption	80uW

5. CONCLUSIONS

A new input architecture of a fully differential successive approximation switched capacitor ADC has been introduced. The cancellation of the VCM buffer and the implementation of the self-timed comparator can reduce the power consumption by the factor 1.5 and doubled the sampling rate at the same time. 100KS/s is guaranteed at worst-case conditions (At 1.8V, temperature 125 C, worst-case process). The resolution was improved from 10-bit to 12-bit. Furthermore, the applicability of the converter in an integrated system was facilitated noticeably because of the reduction of the input and reference capacitance.

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