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# FLEXIBLE VLIW PROCESSOR IMPLEMENTATION ON FPGA AND ITS APPLICATION

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**ABSTRACT**

VLIW processor core implementation on FPGA is now become possible due to high density FPGA available in market. VLIW Processor allows instruction level parallelism (ILP) rather than Execution level which further real time performance can be increased by minimizing development cycle and using common FPGA resource such as larger memory capacity and reconfigurability potential. Applications such as convolution, sound processing, image processing etc. can also be tested and validated. This paper describes research result about enabling the VLIW processor model for real-time processing applications by exploiting FPGA technology.

**Keywords: VLIW instruction, Control Unit ,Lcode generation, VHDL Description, FPGA implementation**

## INTRODUCTION

Emergence of the System-on-Chip (SoC) In the last 10 years increasing technological capacity in area such as process control, telecommunication, satellites, and the medical field. Electronic embedded systems have an important role in it. SoCs have become omnipresent because of the advances in design technology makes SOC omnipresent that means it became possible to build complete systems on same chip having containing different &various components. In this context, the FPGA (Field Programmable Gate Array), a key solution for rapid prototyping of embedded systems is reconfigurability and easy integration capacity. These user programmable solutions are capable of performing the hardware part of a design for a significantly lower price and they maintain many of the advantages of the ASIC (Application Specific Integrated Circuit) solutions. FPGA foundries offer many built-in circuit features, such as memory, multipliers, and high speed communication links. The most interesting characteristic of FPGA, with its reconfigurable nature, is probably the ability to quickly create a rapid and fully functional prototype that can emulate and verify solutions.

## RELATED WORK

Currently, In The Mid 1990s, IC Fabrication Technology Is Advanced Enough To Allow Unprecedented Implementations Of Computer Architectures On A Single Chip. Also, The Current Rate Of Process Advancement Allows Implementations To Be Improved At A Rate That Is Satisfying For Most Of The Markets These Implementations Serve. In Particular, The Vendors Of General-Purpose Microprocessors Are Competing For Sockets In Desktop Personal Computers (Including Workstations) By Pushing The Envelopes Of Clock Rate (Raw Operating Speed) And Parallel Execution. The Market For Desktop Microprocessors Is Proving To Be Extremely Dynamic. In Particular, The X86 Market Has Surprised Many Observers By Attaining Performance Levels And Price/Performance Levels That Many Thought Were Out Of Reach. The Reason For The Pessimism About The X86 Was Its Architecture (Instruction Set).

Indeed, With The Advent Of RISC Architectures, The X86 Is Now Recognized As A Deficient Instruction Set. Instruction Set Compatibility Is At The Heart Of The Desktop Microprocessor Market. Because The Application Programs That End Users Purchase Are Delivered In Binary (Directly Executable By The Microprocessor) Form, The End Users' Desire To Protect Their Software Investments Creates Tremendous Instruction-Set Inertia. There Is A Different Market, Though, That Is Much Less Affected By Instruction-Set Inertia. This Market Is Typically Called The Embedded Market, And It Is Characterized By Products Containing Factory-Installed Software That Runs On A Microprocessor Whose Instruction Set Is Not Readily Evident To The End User. This Lower Level Of Instruction-Set Inertia Gives The Vendors Of Embedded Microprocessors The Freedom And Initiative To Seek Out New Instruction Sets.

The Relative Success Of RISC Microprocessors In The High-End Of The Embedded Market Is An Example Of Innovation By Microprocessor Vendors That Produced A Benefit Large Enough To Overcome The Market's Inertia. To The Vendors' Disappointment, The Benefits Of RICSs Have Not Been Sufficient To Overcome The Instruction-Set Inertia Of The Mainstream Desktop Computer Market. Because Of Advances In IC Fabrication Technology And Advances In High-Level Language Compiler Technology. The New Direction In Microprocessor Architecture Is Toward VLIW (Very Long Instruction Word) Instruction Sets. VLIW Architectures Are Characterized By Instructions That Each Specify Several Independent Operations. This Is Compared To RISC Instructions That Typically Specify One Operation And CISC Instructions That Typically Specify Several Dependent Operations. VLIW Instructions Are Necessarily Longer Than RISC Or CISC Instructions, Thus The Name.

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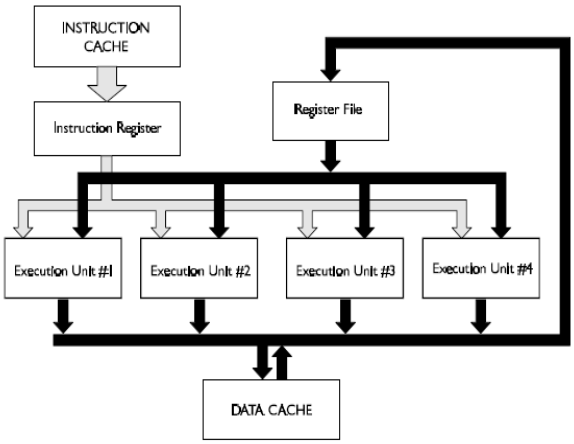


Fig 1: Block Diagram

## SYSTEM DESCRIPTION

Algorithms are first developed on a personal computer in standard programming environment such as In the standard FPGA based prototyping methodology, algorithms are first developed on a personal computer or workstation in standard software programming languages such as C or Matlab. When the algorithm is later implemented in hardware, the C or Matlab code is translated into a hardware description language such as VHDL or Verilog. Finally, the design is synthesized for an FPGA-based environment where it can be tested. Most hardware description languages are inherently concurrent and most high-level software languages are not considered .

One of the key factors that encourage the wide diffusion of electronic devices is the improvement of the man-machine interface, where the great challenge is to allow the use of complex electronic systems by software developers. Many research laboratories and industrial manufacturers are focusing their efforts to that 4 effect . Two major trends emerge. The first, based on the fact that software developers know much more about traditional software high-level programming languages such as C and C++ than about hardware description languages, a major trend consists in extending these languages with variations capable of describing hardware elements. Among the most important, we can find SystemC, HandelC , and Ocapi-XL. These new hardware description languages are, in effect, parallel synchronous programming languages where the notion of time is fundamental to its specification.

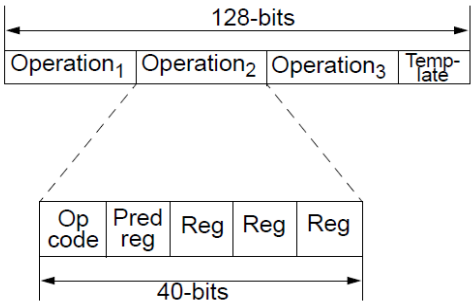


Fig. 2: Instruction Format

In these languages, all events occur relative to a global clock that runs continuously. Information is encoded on a behavioral level in a similar manner to most high level languages. The second trend consists in using single programmable devices. These devices were recently introduced into the market under the name of Programmable System on a Chip (PSoCs).They have a digital programmable section, a microprocessor core, and a programmable analog tile all embedded into them, often together with other specialized modules for communications. In these devices, the embedded microprocessors are high performance CPUs.

## LCODE GENERATION USING OPEN IMPACT COMPILER

The Open IMPACT compiler is maintained by the IMPACT group at the University of Illinois, under the direction of professor Wen-mei W. Hwu. The objective of IMPACT (Illinois Micro-architecture Project utilizing Advanced Compiler Technology) is to provide critical research, architecture expertise, and compiler prototypes for the microprocessor industry. This objective is accomplished by analyzing and demonstrating the level of hardware and compiler support required by architectural enhancements in order to understand the cost and effectiveness of these enhancements. IMPACT's focus has historically been Instruction-Level Parallelism (ILP).

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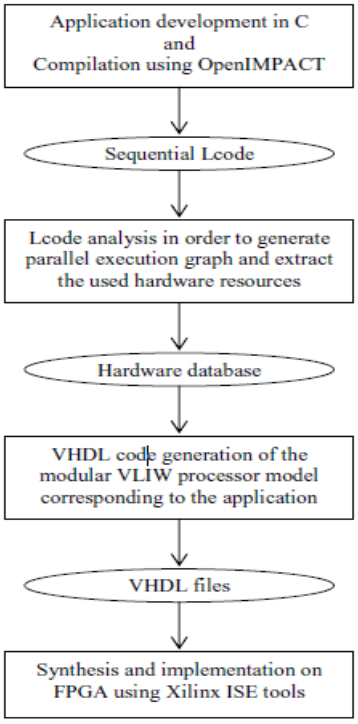
The original source code into an assembly intermediate representation "code" is done using Matlab compile. This produced code is optimized for ILP, but not for a specific machine.




**VHDL DESCRIPTION & FPGA IMPLEMENTATION**

A flexible VLIW processor can be implement using Lcode analysis and graph model generation results. we know minimum need hardware resources for a target application (register number, basic operation types, instruction set and length of each VLIW instruction). we construct the structure of VLIW processor With hardware database information, and VHDL language describe it. It is noted that the VLIW processor is totally customizable and optimal for target application: just minimum necessary functional units, operation types and used registers.

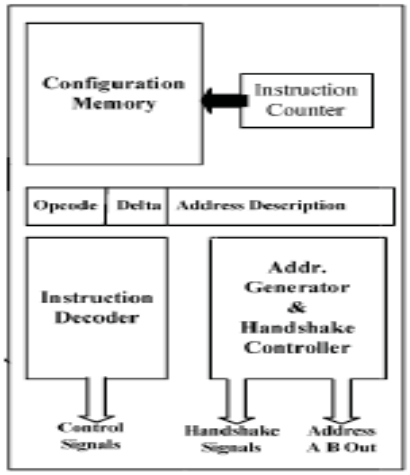



Fig. 4: Control Unit

To present VLIW processor in VHDL language We used a database of hardware templates. to control execution-time scheduling: program fetching, instruction dispatching, and instruction decoding units deliver up to instructions to functional units every CPU clock cycle We respect different pipelined levels of VLIW processors in order. This mechanism has been described in VHDL code and implemented onto an FPGA. All generated VHDL files for a target application have been synthesized using Xilinx ISE 14.7 software tools to realize hardware implementation. simulation result. An implemented design of VLIW PROCESSOR has area utilization frequency as summarized in Table respectively.

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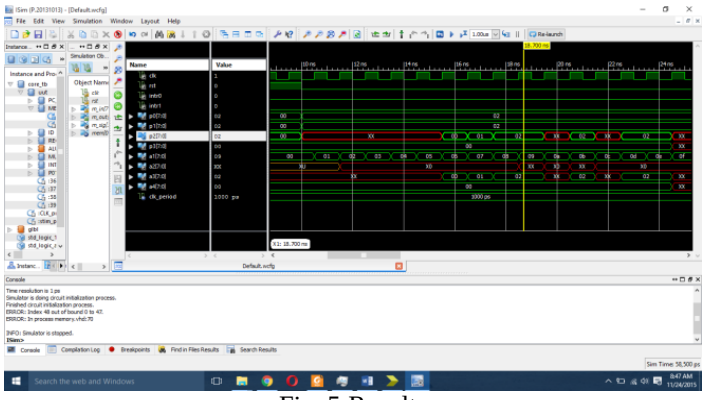

Fig. 5:Results

An overall VLIW PROCESSOR core is implemented using VHDL utilize 704 number of slice register, 3259 slice LUTs, 426 LUT FF pair and 0 number of block RAM used. A maximum 39.591 ns delay with maximum operating frequency 277.693MHz against cost of 0.020 watt total dynamic power at 25.6 0C junction temperature compute using XPower Analyzer tool. Where Figure 5.5 gives a simulation waveform of VLIW PROCESSOR decryption created in Xilinx ISim tool.

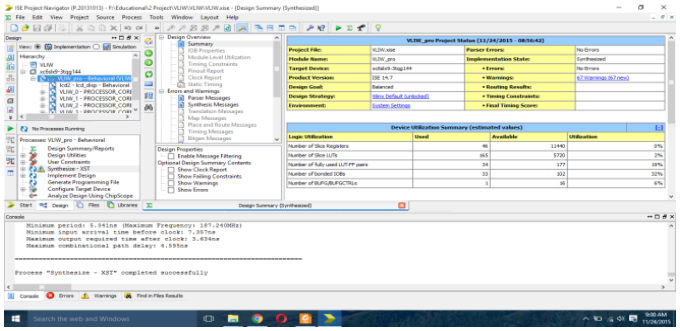

Fig. 6: Power consumption

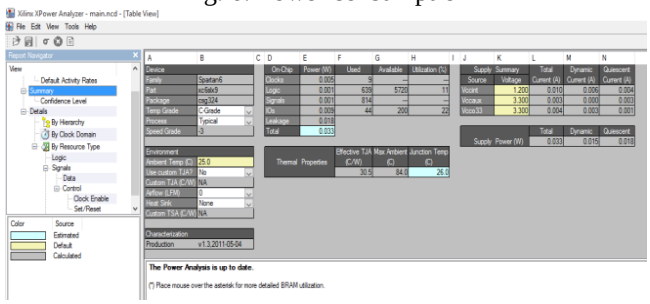

Fig. 7:Design Summary of Proposed Design Core with Existing Change by your result

| Parameter | Proposed Design | [1] | [2] | [3] |
|---|---|---|---|---|
| Platforms | Xilinx Sparton-6 XC6SLX16 | Xilinx Virtex-5 XC5VL50 | Xilinx Virtex-2 XC2VP20 | Altera APEX20K-C |
| Data path (bit) | 128 | 32 | 128 | 128 |
| Area | 554 slices/ 3531 LUT | 769 slices/ 2350 LUT | 9028 slices | 40960 slices/ 895 LUT |
| Frequency (MHz) | 277.693 | 100.8 | 220.7 | - |
| Throughput (Mbps) | 772.95 | 73.3 | 28250 | 1188 |

Table that proposed design also achieves much higher throughput than previous VLIW PROCESSOR encryption designs is summarized in detail

## CONCLUSIONS

The VLWI processor provides a generalized platform for any application program and all the basic arithmetic and logical instructions can be performed. A VLIW Processor contain4 core architecture allows significant saving in the instruction memory size. Up to assembly instructions can be executed using only 1024 x 256

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memory locations. Memory hierarchy does not place any restriction in selecting location to read and write in the memory. There is reduction in the memory size and also the number of resources used. The use of localized RAM gives optimized performance in terms of power, area, and memory access time. This in turn reduces the power consumption and provides a resource efficient processor. Enhanced performance in terms of throughput and resource cost. Thus VLWI processor architecture gives efficient performance in terms of throughput and resource cost. This work can be further extended with the analysis of power and area when considered for ASIC implementation.

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