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HIGHER ORDER MUX BASED VEDIC MULTIPLIER FOR IMAGE PROCESSING APPLICATION

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ABSTRACT

Image Processing is very important in various engineering disciplines. Multiplication is one of the dominant functions in any image processing or DSP application. High speed multiplication is very important in image processing or DSP for matrix multiplication, convolution and Fourier transforms, etc. A less delay and fast method for multiplication based on multiplexer based 8X8 Vedic multiplier is proposed in this paper. The 4x4 mux based Vedic Multiplier is proposed and this is extended to design 8x8 Vedic multiplier using Urdhva_Triyakbhyam Sutra. The coding is done using VHDL and synthesis is done using Xilinx 14.5 on Spartan 6 Board. The proposed multiplier was compared with existing multiplier to obtain minimized delay.

Keywords: Vedic multiplier, multiplexer, shifter, Urdhva_Triyakbhyam, VHDL, Image processing.

1. INTRODUCTION

Vedic mathematics is one of the old systems of mathematics, to be precise, a unique technique of mathematical that depends on some rules and principles to perform any type of calculations that related to the mathematics like arithmetic, geometry, trigonometry and algebra. The method is based on sixteen sutras or algorithms are the simple and easy understandable formulae for solving range of Mathematical problems. Vedic was discovered from old ancient Indian scriptures and it s rediscovered in the year 1911 and 1918 by Sri Bharathi Krishna Tirthaji who studied these scriptures for a years and made many observations and careful investigation then finally able to reconstruct these series of algorithms called sutras. The sutra of Vedic Mathematics are the software for the cosmic computer that runs in the universe many algorithms are discussed among them UT sutra is explained further. Since this algorithm is general for whole number and applicable to any number of calculation. Conventional Vedic Mathematics deals with much simple calculation method on various complicated mathematical problems. The method is totally different and very close to the human mind works. Multiplier design in this paper is based on Multiplexer and Vedic algorithm. Since there is no much complexity in the Multiplexer block which improves the performance further. This Multiplier plays one of the dominant role in the filter calculation for Image processing application.

Kerur et al., [1] proposed multiplier design and used in the Digita signal processing. In this method the sutra from Vedic Mathematics 'Urudhva_Tiryakbhyam' which is applicable to all cases of multiplication was used. The combinational delay is compared with normal multiplier further this is used in the matrix multiplication and concluded that this multiplier improves the performance in the DSP. Pradhan et al., [2] proposed 16x16 and 32x32 MAC (Multiply and Accumulate) unit that includes major components like multiplier and accumulator. The multiplier is designed using Ancient Vedic Technique. A conventional Multiplier and Accumulator that consists sum of previous partial product and used in the DSP processor that enhances the speed of MAC unit. Kokila et al., [3] proposed concepts of 'Urudhva_Tiryakbhyam' and 'Nikilam sutra's of Vedic Mathematics. The 16x16 bit multiplier using Urudhva sutra and Nikilam sutra were designed. The speed and performance evaluation is done on Xilinx platform. Finally concluded that Nikilam sutra best suited for higher order multiplication. The modular design of Vedic mathematics up to 32 bit is proposed in this paper [4], The fast 32x32 multiplier by using 16x16 bit conventional design and also hardware architecture designed found similar to the array multiplier. This is one of the possible applications of Vedic Mathematics to Engineering and serious effort is required to utilize this field for the advancement in the Engineering and Technology. In this paper new method of digit multiplication by higherarchical method was proposed. So the design complexity get reduces as the large number of bits and modularity increased.

Optimized Vedic Technique was introduced in the paper [5], in which they have designed 32x32 bit multiplier using Vedic Techniques. The Urudhva, Nikilam and Anurupye sutras are such algorithm that reduce the power, delay and hardware requirements of any general multiplication. The delay reduction up to 31.56ns for 32 bit was achieved and compared the result with karastuba algorithm which is other technique of multiplier design method. Finally it is concluded that Optimized Vedic technique improves the efficiency.In this paper [6], they have designed multiplier by using Urdhva Tiryambakham and Booth algorithm. The Performance analysis is done. The paper [7], presents the simple method of multiplier design using vedic Mathematics in which it uses 'Urudhva _Triyakbhyam' algorithm for the design of 4x4 and 8x8 multiplier. It is preferred in this design because of its modular and parallel nature of obtaining partial products. Both the design is implemented on SPARTAN-3 which gives the combinational delay of 28.27ns for 8x8 bit multiplier.

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The design of 8x8 bit multiplier and implementation on chipscope-VIO is proposed in this paper [8]. In this Vedic multiplier and square of 8 bit is desined. Due to timing efficiency, less delay and high speed ,the proposed Vedic multiplier and square design is used in ALU replacing the traditional array and BOOTH multiplier. The paper [9], gives a novel architecture of 32 bit floating point multiplier using Vedic Mathematics Technique. The Mantissa multiplication uses 'Urudhva_Triyakbhyam' sutra. The overflow and underflows are handeled in this paper. The 24x24 bit floating point multiplier is designed and implemented on vertex device. Efficient use of Vedic method is shown here and lesser number of LUTs shows that the hardware requirement is reduced. Arepetative and regular structure of Vedic technique makes it easier to design of multiplier. The complex Multiplier is presented in the paper [10], which uses Very popular the vedic Technique. The 'UT' is proposed for multiplier design because of its one of the advantage like the sums and partial products are generated in one step in which it reduces the time of propogation from LSB to MSB. To decrease the number of multiplication and to increase the speed complex multiplier is designed. Since may real time DSP applicatios requires number of complex multiplication in which high performance is the main target. The UT sutra gives less number of bits to implement high speed complex multiplier. Introduction of this multiplier helps a lot to design complex number design of higher bits.
The multiplier design using Vedic Mathematics proposed in the paper [11], in which 'Urudhva_Triyakbhyam' is used and carry look ahead adder (CLA) is used instead of general ripple carry adder (RCA).This carry look adder is faster than in terms of execution speed since it reduces the amount of time required to determine carry bits. This adder will generate the carry before the sum which reduces the wait time to calculate the result of larger bits. This adder depends on two things one to calculate each digit position that propagate carry and other thing combining allthese calculated values and finding whether the group is propagating carry. The multiplication speed of this multiplier is high because of Vedic Mathematics and the addition time is also increased by using this type of adder.

2. PROPOSED TECHNIQUE

The URUDHVA_TRIYAKBHYAM (UT) is one of the most popular and general algorithm among sixteen sutras of Vedic mathematics. This is due to it can be applied to all type of numbers (higher or lower order). In the Sanskrit Urudhva means vertical and Triyakbham means crosswise.

The steps for Multplication is given below

Step-1: Vertical multiplication of least significant bits of two binary numbers-M0XN0 =0x0=0, it is the least bit
of partial product P0 with carry 0(C0).
Step-2: Next crosswise multiplication of M1XN0+M0XN1 = 0X0+1X1+C0= 1(P1) with carry 0(C1).
Step 3: Next vertical and crosswise multiplication of M0XN2+N0XM2+M1XN1+C1 = 1X1+ 0X0+0X1+0=1(P2) with carry 0(C2).
Step-4: Similarly M0XN3+M3XN0+M1XN2+M2XN1+C2=1X0+1X0+0X1+0X1+C2=0(P3) with carry 0(C3).
Step-5: M1XN3+M3XN1+M2XN2+C3=0X0+1X1+0X1+0=1(P4) with carry 0(C4).
Step-6: M2XN3+M3XN2+C4=0X0+1X1+0=1(P5) with carry 0(C5)
Step-7:M3XN3+C5=1X0+0=1X0+0=0(P6) with carry 0(C6).

Finally the output is C6P6P5P4P3P2P1P0=00110110
Example product of (M3M2M1M0)1001 and (N3N2N1N0)0110

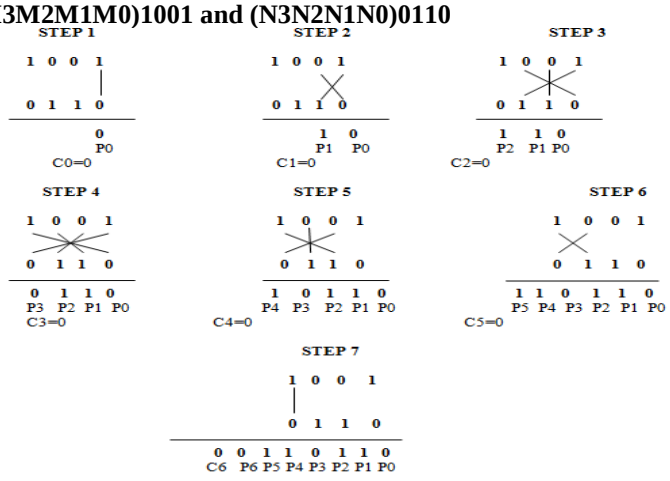

Fig 1. Urdhva Tiryambakhm Algorithm

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2.1 DESIGN OF 4X4 MUX BASED VEDIC MULTIPLIER

The 4x4 muxvedic multiplier design consist of shifters (shift left by 1, shift left by 2,shift left by 3), adders and one 16x1 multiplexer. In this multiplier is taken as select lines of multiplexer and multiplicand as input to the shifters. Depending upon select line corresponding input passed to the output and there is no complexity in the design. The input is 4 bit and ouput is also of four bit.

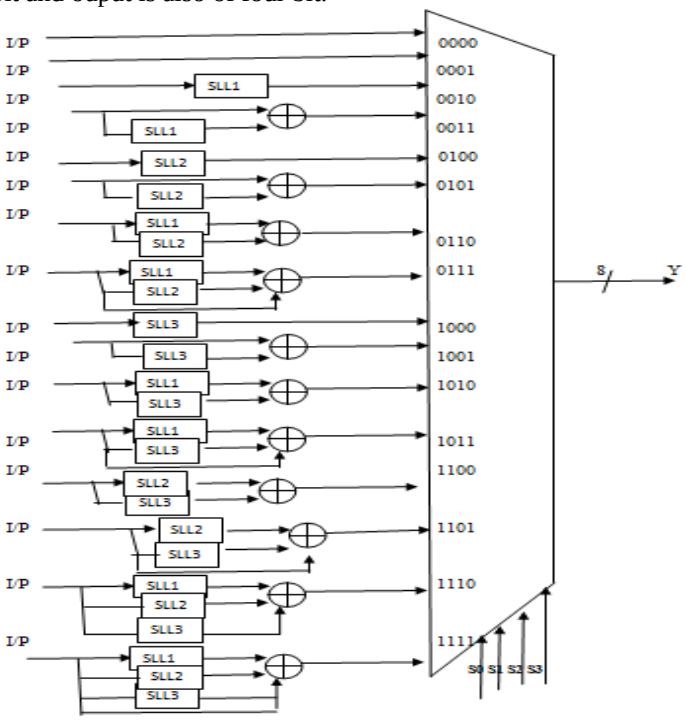

Fig 2. 4X4 MUX Based Vedic Multiplier

2.2 DESIGN OF 8X8 VEDIC MULTIPLIER USING 4X4 MUX BASED VEDIC.

The proposed multiplier uses the above designed 4x4 MUXVEDIC to perform 8x8 bit multiplication.

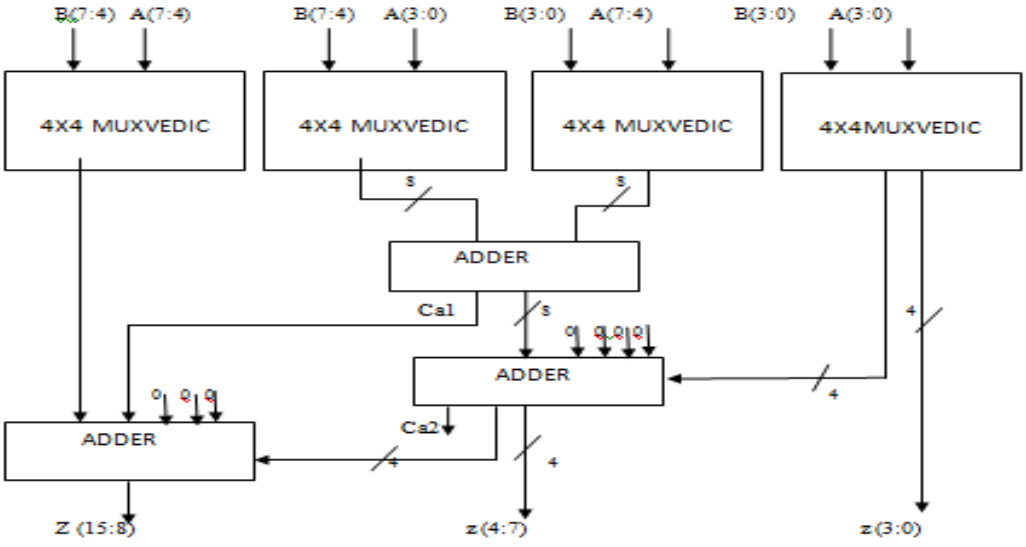

Fig 3. 8x8 MUX Based Vedic Multiplier

2.3 ARCHITECTURE FOR IMAGE PROCESSING APPLICATIONS

The proposed 8x8 MUXVEDIC is used in the convolution for smoothing of noisy Image input as shown in Fig 4 where the image pixel values are convolved with the filter coefficients using proposed vedic multiplier and the filterd output are stored in memory using D flip flop.

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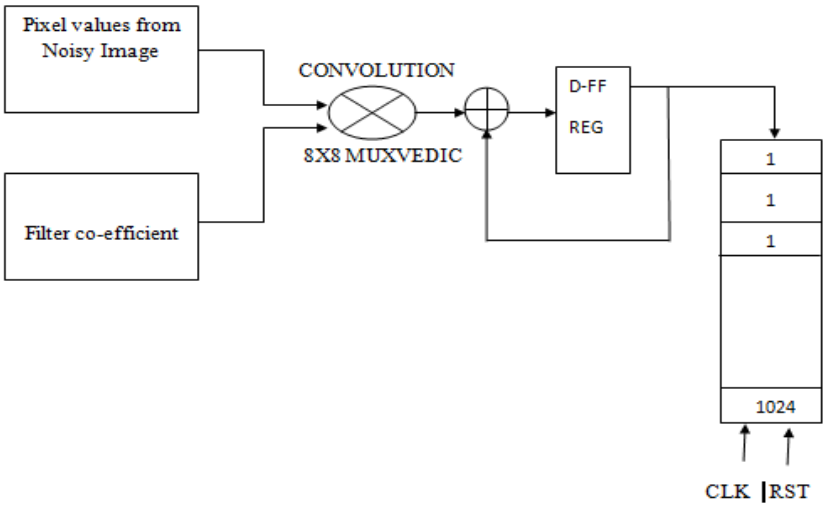


Fig 4. Architecture For Filtering Using Proposed Vedic Multiplier

3. RESULTS AND DISCUSSIONS

3.1 RTL SIMULATION AND OUTPUT WAVEFORM OF 4X4 MUXVEDIC

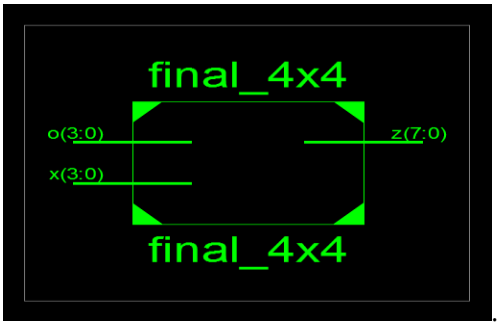


Fig 5a. RTL OF 4X4 MUXbased Vedic

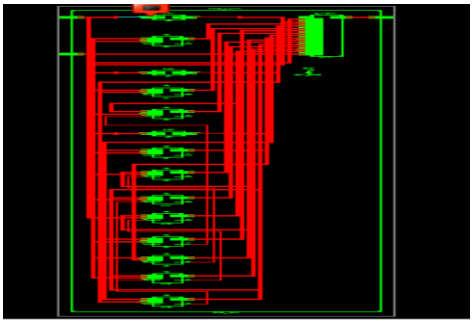


Fig 5b. SimulationOF 4X4 MUX Based VEDIC

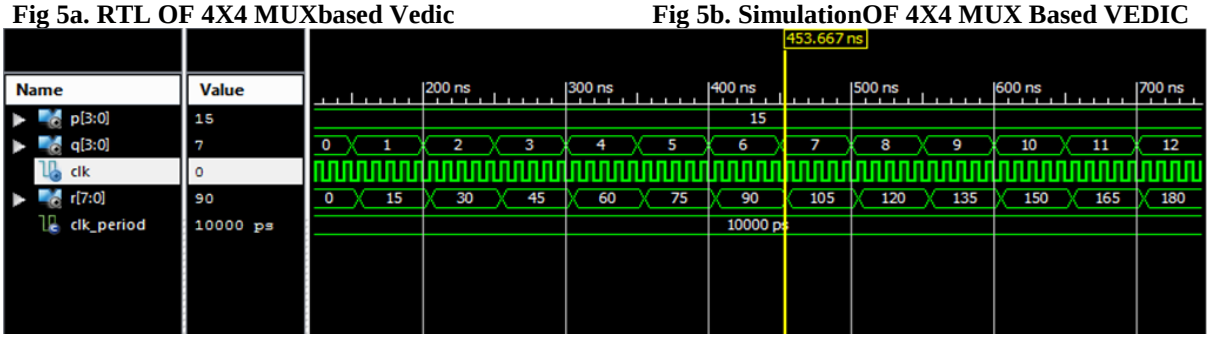
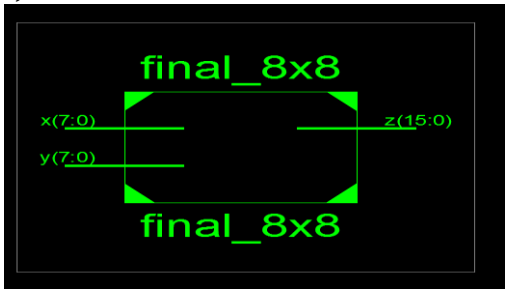


Fig 5c. Output Waveform OF 4X4 MUX Based Vedic

The RTL consist 4 bit of two input and 8 bit of one output in the Fig 5a, Fig 5b gives corresponding simulation results and Fig 5c gives output in the waveform nature.

3.2 RTL, SIMULATION AND OUTPUT WAVEORM OF 8X8 MUXVEDIC



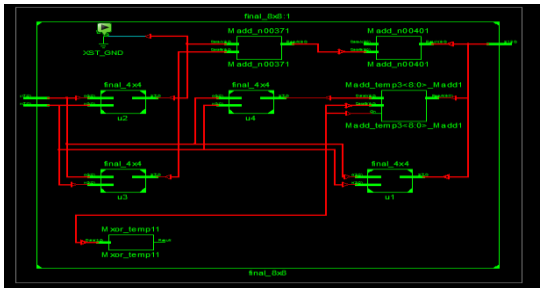


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Fig 6a RTL OF 8X8 Vedic Multiplier **Fig 6b Simultion of 8X8 Vedic Multiplier**

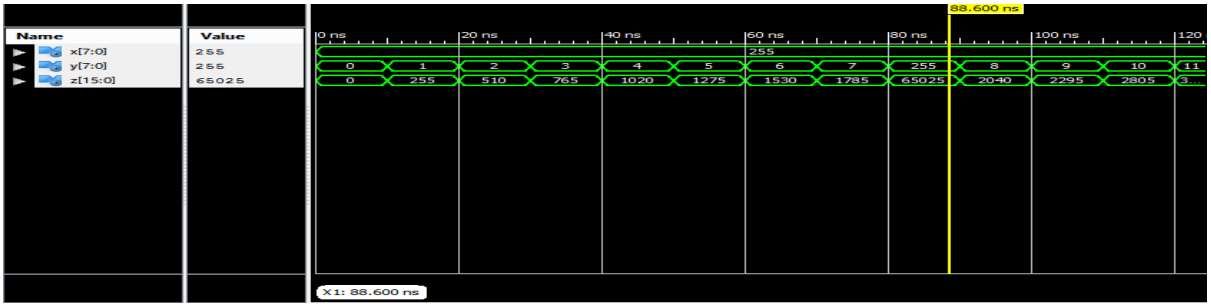

Fig 6c Output Waveform of 8X8 Vedic Multiplier using 4x4 MUX based Vedic

The Fig 6a gives the RTL of 8x8 proposed MUXVEDIC, Fig 6b gives corresponding simulation and synthesis results and Fig 6c gives the output.

TABLE 1: DELAY COMPARISION OF 8X8 EXISTING AND PROPOSED DESIGN
DEVICE:3S50ATQ144-5

AUTHOR	MULTIPLIER	M X N	DELAY
Satish S Bhairannawar et al., [12]	MUX Based	8X8	20.008ns
Proposed Method	MUX Based	8X8	17.621ns

The Proposed MUX based multiplier was compared with existing MUX based multiplier proposed by Satish S Bhairannawar et al., [12] and was it observed that the proposed method delay is less compared to existing multiplier since, the proposed method uses 4x4 mux based design compared to 2x2, 3x3 and 3x2 mux based in existing techniques.

4. CONCLUSION

Vedic Mathematics is the symmetric computation which performs the various Mathematical calculations like arithmetic, trigonometry, geometry, calculus etc. All sutras in Vedic are very efficient and understandable when compare to manual calculations. The proposed 8x8 Mux based Vedic Multiplier designed achieved less delay when compared to existing Mux based Vedic multiplier [12] i.e., approximately 10% reduction in delay compared to referenced paper. The proposed multiplier was used in the Image processing application to obtain filtered output.

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