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Energy efficient MOS digital circuit for low power VLSI design

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ABSTRACT

Recent advances in CMOS VLSI design reduce device size and due to this, the minimization of energy dissipation has become a primary critical concern. In order to design portable systems, we introduce an idea for low power and high speed switching that is adiabatic strategy which minimizes the power consumption by regaining energy drawn from the supply clock. In this paper, all work is done using SPICE tool to simulate results of the proposed technology and other strategies also; these results show empirical comparison between different parameters such as logic style, power dissipation and delay. A minimum dissipation of the energy at a certain frequency is observed i.e. an optimum frequency exists in adiabatic logic where energy consumed per cycle is minimized. These improvements show that proposed method can considerably reduce the power consumption in new design when compared to the conventional CMOS design techniques.

Keywords*: Adiabatic logic, efficient charge recovery, Low power, Power clock*

1. INTRODUCTION

Demand for low power and high speed digital circuits has motivated VLSI designers to explore new approaches in the field of designing VLSI circuits. Also, the thermal stress caused by power dissipation as heat, on chip is a major reliability issue. Therefore, reduction of power dissipation is also desirable for reliable enhancement. Energy recovery (adiabatic) logic is a promising approach, which has been originally developed for low power digital circuits [1]. Systems having switching activities, dynamic power is a dominant factor in energy dissipation. In conventional CMOS circuits, energy dissipation can be minimized through adiabatic technique and some of energy stored in load capacitance can be reused instead of dissipated as heat [2].

The term "Adiabatic" was firstly coined at the Second Workshop on Physics and Computation in this context appears to be in 1992. Although researcher has made an earlier suggestion about energy recovery where in relation to the energy used to perform computation, "This energy could in principle be saved and reused". There are some classical methods to reduce the dynamic power dissipation such as decreasing voltage power supply, reducing physical capacitance and reducing switching activity [3]. These techniques are old and not enough to meet desired power requirement in present condition. Hence, most research has been focused on building adiabatic logic. Adiabatic logic works with switching activities which reduces the power by giving stored energy back to the supply [4]. Hence, the term adiabatic is relevant for low power VLSI design circuits, which implements reversible logic. Generally power supplies of adiabatic logic circuits have used constant current source to get this, while non-adiabatic circuits that have used fixed-voltage power supply.

2. FOUR MAIN COMPONENTS OF TOTAL POWER DISSIPATION

Total power dissipation of a CMOS Circuit is given by

i) Dynamic (switching) power dissipation: $P_{dynamic}$ is the dynamic switching power which dissipates when charging or discharging of the parasitic capacitances occurs during a node voltage transition.

ii) Leakage power dissipation: $P_{leakage}$ is a combination of MOSFET switches and gate leakage power caused by carrier tunneling through thin gate oxides.

iii) Short-circuit power dissipation: $P_{short-circuit}$ is the transitory power dissipation during an input signal transition when both the pull-up and pull-down network of CMOS gate are simultaneously on.

iv) Static power dissipation: P_{DC} is the static DC power consumed when a CMOS circuit is driven by low voltage swing input signals.

3. DYNAMIC POWER DISSIPATION

Charge-up phase: Output voltage rises from zero to V_{DD}. Fifty percent of energy taken from supply is dissipated as heat through PMOS and rest is stored in load capacitance.

Charge-down: Output voltage drops from V_{DD} to zero. Load capacitance energy is dissipated as heat through NMOS [5, 6].

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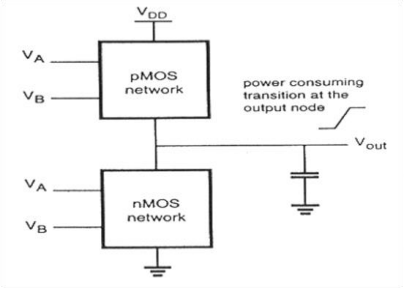

Figure 1. General CMOS circuit [2]

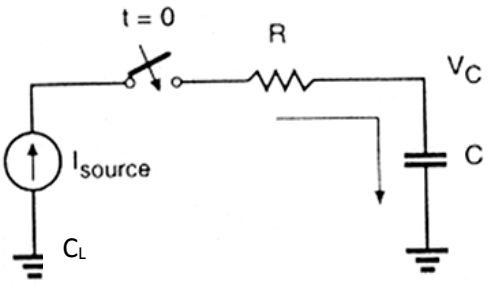

Figure 2. Equivalent circuit for adiabatic switching [2]

General CMOS circuit having NMOS network, PMOS network and total output load capacitance is shown in Fig. 1 [2]. The average dynamic power dissipation for this network is given as:

$$P_{avg} = \left(\sum_{i=1}^{\#\ of\ nodes} \alpha_{Ti} C_i V_i \right) V_{DD} f_{CLK}$$

Where, α_T Switching probability, V_i the node voltage, V_{DD} the full voltage swing, C_i is the parasitic capacitance linked with each node in the circuit (including the output node) and α_{Ti} represents the corresponding node transition factor associated with that node [2].

4. ADIABATIC LOGIC

In conventional CMOS logic circuits with rail to rail output voltage swing, each switching event causes an energy transfer from the power supply to the output node [2, 7]. Depending on the input signal, in steady state either PMOS device or NMOS device is on, the remainder is off. If an input signal transition from 1 to 0 occurs, energy is drawn from the power supply at a constant voltage to charge the output capacitor to the voltage V_{DD}. A charge of $Q = C_{load}V_{DD}$ is taken from the voltage source, an energy quantum of $E_{supply} = QV_{DD} = C_{load}V^2_{DD}$ is drawn from the power supply during this transition. The difference between the delivered energy and the stored energy is dissipated in the PMOS network. If an input signal switches from 0 to 1, in steady state, NMOS is on and PMOS is off. Charge stored on output capacitance is then dissipated via the NMOS network to ground.

To reduce the power dissipation we can minimize switching activities or load capacitance or voltage swing or apply a combination of these three. For making energy efficient logic circuits, the concept of adiabatic logic can be introduced for energy recovery [8, 9].

4.1 Adiabatic Switching

Fig. 2 shows a circuit for adiabatic switching where a constant current source equivalent to linear voltage ramp is used to charge the load capacitance instead of using constant voltage source. In circuit resistance R is equivalent to the ON resistance of PMOS network. Energy can be transferred to the load capacitance through the power supply using constant current charging process. By adiabatic operation it is possible to allowing the stored charge from the load capacitance back to the power supply by reversing the current source direction. For this constant current source must be capable to retrieve the energy from the load capacitance. Hence adiabatic logic circuits require pulsed power supply [2, 10].

4.2 Adiabatic Logic gate

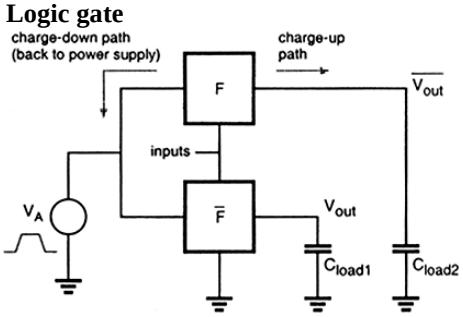

Figure 3(a). Conventional CMOS logic gate [2]

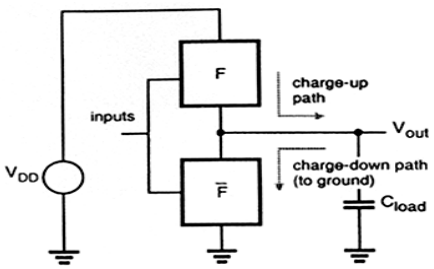

Figure 3(b). The topology of an adiabatic logic gate implementing the same function [2]

The conventional CMOS logic gate and adiabatic logic gate are shown in Fig. 3(a) and Fig. 3(b) respectively. A conventional CMOS logic gate can be converted into an adiabatic logic gate. For this, pull-up and pull-down networks of the conventional CMOS logic circuits must be changed with complementary transmission gate networks [11].

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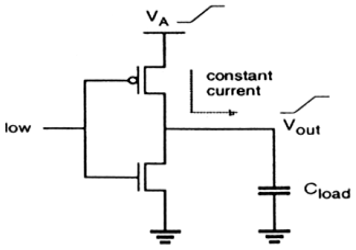

Figure 4. A CMOS inverter circuit with a stepwise increasing supply voltage [2]

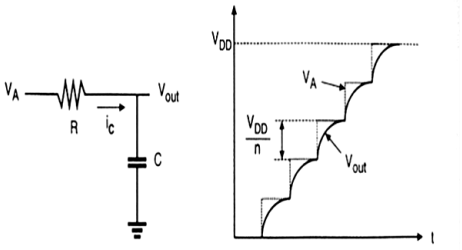

Figure 5. Equivalent circuits and the input and output voltage waveforms of the CMOS inverter circuit [2]

A CMOS inverter is shown in Fig. 4. This circuit uses a stepwise voltage ramp V_A as a power supply having n equal voltage steps as shown in Fig. 5. When supply rises from zero to V_{DD} , the load capacitance is charged through a resister (ON resistance of PMOS) in small voltage increments. Therefore, the total energy dissipation (hence total power dissipation) is reduced by a factor using stepwise charging. If n approaches infinity i.e. if supply voltage is a slow linear ramp, the energy dissipation will approach zero.

5. DIFFERENT LOGIC FAMILIES

Practical adiabatic families can be classified as either partially adiabatic or fully adiabatic. In a partially adiabatic logic circuit, some charge is allowed to be transferred to the ground. In a Fully Adiabatic, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face problems with respect to operating speed and input power clock synchronization. Complete recovery of the power-clock is not possible through the PMOS device, so it is still only a quasi-adiabatic logic style [12].

Many researchers have proposed techniques, methods or models for energy efficient CMOS digital circuits. We found the following, are the noteworthy contributions in the field of proposed work.

5.1 Efficient Charge Recovery Logic (ECRL)

Fig. 6(a) shows the schematic of the Efficient Charge Recovery Logic (ECRL). A detailed description of ECRL can be found in [10, 13, 14]. Full output voltage swing is obtained because of the cross-coupled PMOS transistors in both, pre-charge and recover phases. But due to the threshold voltage of the PMOS transistors, circuit suffers from the non-adiabatic loss in both, pre-charge and recover phases.

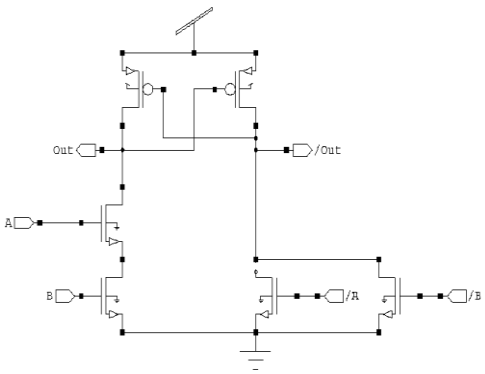

Figure 6(a). Structure of the Adiabatic ECRL Logic

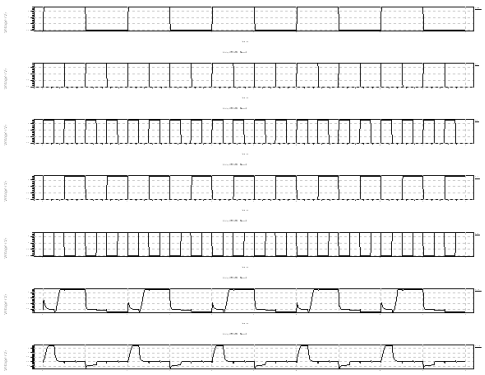

Figure 6(b). Simulated waveforms of ECRL

5.2 2N-2N2P Adiabatic Logic

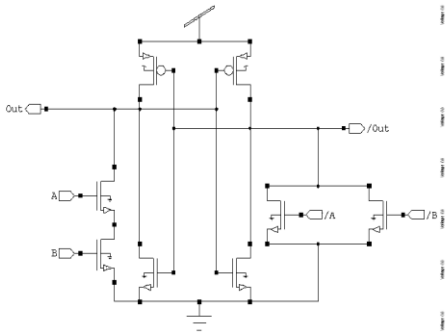

Figure 7(a). Basic Structures of the Adiabatic 2N-2N2P Logic

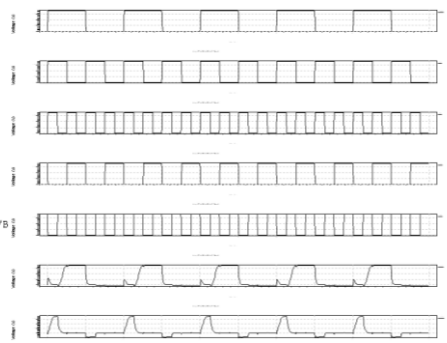

Figure 7(b). Simulated waveforms of 2N-2N2P Logic

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This was proposed as a modification to ECRL logic, in order to reduce the coupling effects. Fig. 7(a) shows the general schematic of the 2N-2N2P logic [11, 15, 16].
The 2N-2N2P logic uses a cross-coupled latch of two PMOSFETs and two NMOSFETs. The primary advantage of 2N-2N2P over ECRL is that the cross- coupled NMOSFETS switches result in non-floating outputs for large part of the recovery phase. It can be seen that at the non-adiabatic loss is dependent on the load capacitance. A more detailed explanation of 2N-2N2P adiabatic logic family can be found in [11].

5.3 Proposed logic

In CMOS circuits, active power dissipation depends on voltage swing, node capacitances and the switching activity of the circuit (number of transitions occurred per second) which depends on the frequency of operation. Fig. 8(a) shows the general schematic of the proposed logic. Proposed research work is based on circuit level approach to minimize power dissipation in MOS circuit, in which energy loss is reduced by limiting voltage differences across conducting devices. We ensure that the voltage drop across the transistor is relatively small at the time when the switching occurs. This is accomplished by using time varying voltage waveforms. A minimum dissipation of the energy at 500 MHz clock frequency is observed. Therefore an optimum frequency exists in adiabatic logic, where energy consumed per cycle is minimum.

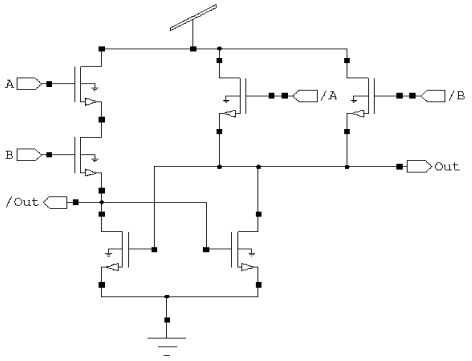

Figure 8(a). Proposed circuit

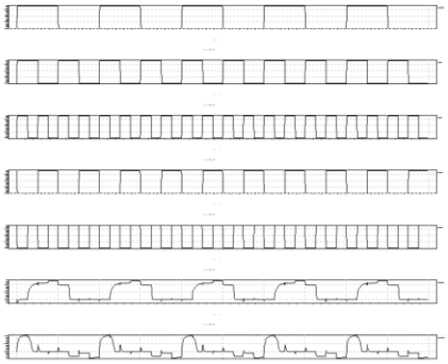

Figure 8(b). Simulated waveforms of proposed logic

6. RESULT AND DISCUSSION

The proposed logic circuit is designed based on 180 nm technology and is simulated using SPICE tool. Power clock supply is 1.8V. Evaluation of the performance of proposed logic in terms of power consumption and delay is given in table 1. ECRL and 2N-2N2P logic based NAND gates are also designed and simulated for comparison. Power consumed and delay by three technologies at operating frequency 500MHz are shown in Fig. 9(a) and 9(b) respectively.

TABLE 1: POWER AND DELAY OF TECHNOLOGIES

Logics	Frequency 500MHz	
	Average power consumption	Delay
Proposed	5.5e-05	3.5e-10
ECRL	1.03e-04	3.6e-10
2N-2N2P	1.3e-04	3.9e-10

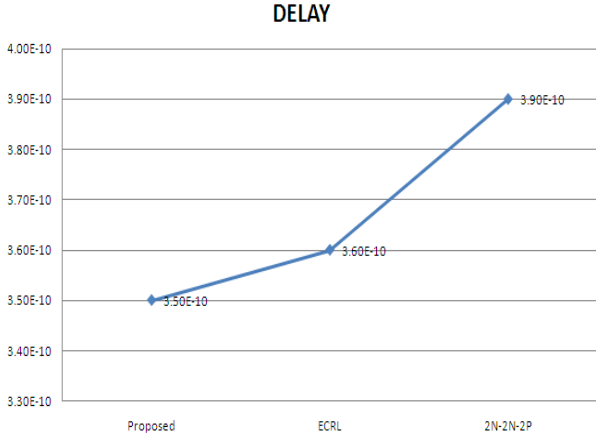

Figure 9(a). Comparative analysis of Power consumption

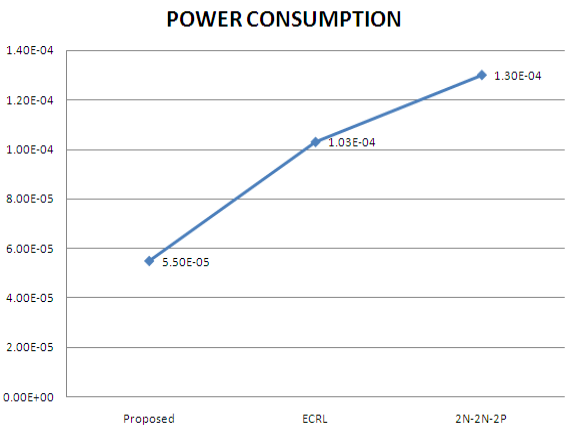

Figure 9(b). Comparative analysis for delay

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7. CONCLUSION

In this paper energy efficient NAND gate based on ECRL, 2N-2N2P and proposed logic is presented. The proposed logic exhibits considerable improvement in terms of power dissipation and delay compared to ECRL and 2N-2N2P technology.

In summary, proposed logic can provide useful building block in design of energy efficient circuits.

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